DESIGN, DEVELOPMENT AND IMPLEMENTATION OF A NOVEL FOUR SWITCH INFINITE LEVEL INVERTER

Thesis submitted to

UNIVERSITY OF CALICUT

In fulfillment for the award of the degree of

DOCTOR OF PHILOSOPHY

By

AJMAL K.T.

Department of Electrical Engineering

Government Engineering College, Thrissur

University of Calicut

September 2020

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Certificate

This is to certify that the thesis entitled ***"DESIGN, DEVELOPMENT AND IMPLEMENTATION OF A NOVEL FOUR SWITCH INFINITE LEVEL INVERTER."*** *is the record of bonafide research work done by* ***Mr. Ajmal K.T.*** *under my supervision and guidance at Department of Electrical Engineering, Govt. Engineering College, Thrissur in partial fulfillment of the requirements for the Degree of Doctor of Philosophy under the Faculty of Engineering, University of Calicut.*

Thrissur-9 ***Dr. JAYANAND B.***

24.09.2020

DECLARATION

I ***Ajmal K.T.,*** *hereby declare that the thesis entitled "****DESIGN, DEVELOPMENT AND IMPLEMENTATION OF A NOVEL FOUR SWITCH INFINITE LEVEL INVERTER****." is based on the original work done by me under the guidance of* ***Dr. Jayanand B****., Professor, Department of Electrical Engineering, Govt. Engineering College, Thrissur for the award of Ph.D. programme under University of Calicut. I further declare that this work has not been included in any other thesis submitted previously for the award of any Degree, Diploma, Associateship or Fellowship or any other title for recognition.*

Thrissur-9 ***AJMAL K.T.***

24.09.2020

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Abstract

Most of the industrial applications and renewable power extraction schemes require inverters for the energy conversion and grid integration purpose. Among the various inverter topologies available, Multilevel Inverter (MLIs) has emerged as a very promising topology for medium voltage applications. MLIs are used extensively in the medium voltage drive applications, Flexible AC transmission systems, and power quality enhancement circuits and for renewable power extraction. Improvement in the output quality with voltage level increase is the major attraction of the multilevel inverters. But, with the increase in the number of voltage levels, the number of switches required also increases. The number of sources–and the number of capacitors or diodes also get increased in this process. Also, the utilization of available DC bus voltage is limited for MLIs. A new concept of infinite level inverter (ILI) was introduced which is having advantages over conventional ILIs. Unlike conventional MLIs the output voltage level of ILI depends upon the switching frequency. As the frequency is very high the output voltage levels will also be high approaching infinite levels. There is no increase in the number of switches, capacitors or inductors in the case ILI. The output voltage is having very low THD, less than 2% with a switching frequency of 10 kHz and with the given parameters. For three phase ILI topology, the DC bus utilization very high. Motivated from the Infinite Level Inverter topologies, and to improve the outcomes of the topology further, a novel Four Switch Infinite Level Inverter (FSILI) having reduced number of switches, improved harmonic performance with the same DC bus utilization is proposed in this work.

The main focus of this work is to design the proposed novel Four Switch Infinite Level topology and then to develop and implement it to understand its characteristics. A three phase Four Switch Infinite Level Inverter topology is derived from the proposed FSILI topology which is having high DC bus utilization along with high output quality and reduced switch count. Closed loop control of proposed FSILI is done with current control and voltage control methods. Grid tied operation of proposed FSILI is also investigated and a modified current control method is used for modulating the active power injected to utility grid. The grid integration of the inverter is successfully achieved in the simulation environment. To validate the theoretical concept of proposed FSILI, a laboratory prototype is setup and the results are obtained in line with the theory and simulations.

The main objectives of this research can be enumerated as follows

- To analyze the performance of conventional Infinite Level Inverters.
- To propose a Novel Four Switch Infinite level Inverter having low harmonic distortion and to perform its
    - Steady state analysis and design.
    - Simulation study and result analysis.
    - Hardware Implementation and result validation.
- To introduce a Novel Three phase Infinite level Inverter topology with reduced number of switches and thus
    - To analyze the DC bus utilization under different modulation techniques
    - To compare the performance of the proposed Three Phase FSILI with the existing topologies

- To propose a grid tied Four Switch Infinite Level Inverter topology with modified current control technique capable of controlling active power injected onto grid.

The first phase of the research work is concerned with the comparison of existing inverter topologies based on the quality of output voltage and the number of switches in the circuit. The inverters employed for renewable power extraction and for other applications were studied. Multilevel inverters were analyzed on the basis of the number of switches, capacitors and sources. Infinite Level inverter topology as an advancement in the multilevel topologies is investigated. The circuit consists of a front end buck converter followed by an H-Bridge inverter. Output of the ILI has minimum harmonic content of the order of less than 2%. The three phase ILI topology has high DC bus utilization. Circuit and result analysis give the inference that the topology has an additional high frequency switch and diode which can be eliminated with certain modifications. Also, the use of separate H-bridge brings additional distortions at the zero crossing instances.

In the second phase of the research work a new inverter topology named Novel Four Switch Infinite Level Inverter is proposed to overcome the shortcomings of the conventional ILI topology. The topology has only four switches and among the switches only one operates at high frequency at a time reducing the switching loss to the possible minimum level. The topology has very low THD of the order of 0.5% which is a key feature. Reduction in the number of switches results in reduction in cost, weight and also the losses. The design, steady state analysis and simulation of the Novel FSILI are carried out. An experimental prototype of the proposed FSILI is also setup in the laboratory and the theoretical and simulation results are validated.

In the third phase of the research work, a Three Phase Four Switch Infinite Level Inverter is derived from the single phase Four Switch Infinite Level inverter. The topology is having high DC bus utilization just same as the conventional three phase ILI. Number of switches is reduced and thus the size and cost of the inverter also reduced. The quality of output obtained is high in comparison with the conventional three phase ILI. Here the line voltage THD is obtained to be less than 0.5% which indicates that the topology can be a solution for critical applications. The harmonic analysis for different load conditions is also done and the results are compared with conventional ILI.

Novel FSILI is further analyzed for its use in the renewable power extraction and grid integration. A current control method for the grid tied operation of the proposed FSILI is proposed which is based on hysteresis control. A grid synchronization technique without PLL is also discussed. The simulation study is carried out with proposed current control technique for both islanding mode and grid tied mode. The proposed grid control method is capable of controlling the power injected onto grid. Unity power active power injection is achieved for different power levels. In islanding mode also the transient response with sudden change in the reference variations is found to be satisfactory. The current injected is analyzed for the THD and it is obtained as well within the IEEE standards.

Contents

List of Figures

List of Tables

Chapter I

INTRODUCTION

Electrical Energy is one of the cleanest forms of energy available in earth. It is very easy to carry electrical energy from one location to other, making it a medium of energy transfer. The energy requirement of the world is increasing exponentially day by day. Fossil fuels, one of the major sources of energy for the past century is now becoming least reliable since it gets depleted day by day without a chance for immediate replacement. So, the main focus is now on finding new sources of energy which won't die out in the near future. Such sources should be reliable, pollution free and should be easily extractable. Such Renewable energy sources (RES) will not produce greenhouse gases and are abundant in nature.

Solar Photovoltaic, Wind, Hydro electric, geothermal etc are some of the RES which can be utilized to meet the tremendous energy requirement of the world. The effective methods to efficiently tap these RES are the challenge the researchers address today. Extraction of power from these renewable energy sources with the maximum possible efficiency is achieved with the invent of power electronic converters. Power electronic converters are the heart of the energy extraction system. With a proper control implementation the losses can be minimized.

Power electronics is the state of the art technology which revolutionized the power processing sector. Power electronic converters are used in various applications ranging from Aerospace to the house hold systems. With the advancement in the semiconductor technology and controllers the size and complexity of the power electronic systems reduced drastically. The different available forms of electrical energy are converted in to the desired form with the help of these power electronic converters. The various power processing operations carried out using the power electronic converters include rectification, inversion, DC -DC and AC-AC conversion. These operations are application specific and are used in the industry quite extensively.

The DC-AC conversion or inversion is essentially one of the major power processing operations. The power electronic converter used here is termed as Inverter. Since most of the end loads in an electric system works on AC, the inverters are gaining very much importance these days. In house hold commercial systems uninterrupted power supply systems are realized with the help of inverters. In industries the process control operations require adjustable speed drives and most of them are induction motor drives. The speed and torque control of these ASDs are very important for the industry.

Other important aspect the inverters became most popular in industry is the requirement emerged in terms of power extraction from the available renewable energy sources. The renewable sources like solar, fuel cell etc. will produce electrical energy in the direct current (DC) form. There can be intermediate DC-DC converters for these RES to stabilize the voltage level while the extraction is being done. Since, the utility grid is commonly AC in nature and the loads employed are designed to operate with alternating current, an inverter is essential in the process of power extraction from renewable sources. Apart from that, in wind energy systems, the commonly used wind generators are induction generators. The electricity produced from wind energy conversion systems are AC in nature but is with variable frequency. Before integrating this AC power on to the grid, the frequency should be converted into grid frequency. The most common practice is to convert this variable frequency AC into DC and then to convert back to fixed frequency ac voltage using an inverter. Thus, it can be seen that, the extraction of power invariably requires inverters with adequate control strategies to perform the required task.

The power extracted from the distributed generators (DGs) can either be integrated on to the utility grid or can be used in the stand alone mode. In the micro grid and nano grid systems, these distributed generators produce the electricity and will be delivered to the loads in the same grid. The concept of DC micro grid is in the growing stage but the common system is AC grid system. So, in order to ensure the required voltage and frequency suitable for the operation either in the micro, nano or the utility grid system inverters are integrated along with these RES.

The grid tied operation is very essential for many reasons which obviously include meeting the global energy demand with the possible sources of energy and to maintain a standard system voltage and frequency specified by the end user loads. Also, the grid connected inverters connected along with passive capacitors will act as active power filter circuits or STATCOM as per the requirement. The active power filter will compensate for the harmonic currents. STATCOM will deliver reactive power and will maintain the reactive power profile of the grid. Further, the grid integration will ensure active power control with the help of advanced grid control algorithms. These grid power control and harmonic control are very much essential since most of the loads need quality power for the proper operation.

In automotive applications, the commonly used electric motors are PMSM, BLDC and IM. From the battery storage system, the power is being delivered to the load with the help of inverters. In the case PMSM and IM, pure sinusoidal output is essential for smooth torque production.

It can be understood that the DC-AC inverters are the key player in modern electric systems with its application ranging from house hold UPS systems to the automotive sector. The Power extraction invariably requires inverters with advanced grid control techniques. The extensive use of power electronic DC-AC inverters invited the attention of researchers to do more on the investigation of new effective, efficient and cost effective inverter topologies. The advancements in the field of device manufacturing technologies, the invention of new digital controllers and the introduction of more efficient control algorithms paved the way to new inventions in the DC-AC inverters.

Quality of the inverter output should be ensured in the conversion process so as to cope up with the load requirement. Harmonic Factor, Total harmonic distortion, power factor etc. are some of the measures to understand the power quality of the inverter output. As per the IEEE standards, the THD should be less than 5% in the distribution network. For the grid integration also, the THD should be as low as possible. The power factor depends upon the nature of load but the injected power can be made with unity power factor with the help of grid control techniques. For ensuring proper grid power quality, the reactive power control can also be implemented. The research focus on how to

mitigate the power quality issues and how to ensure distortion free AC supply available for the loads give light in to introduction of new inverter topologies and advanced control techniques.

Most common and first in the queue of inverters are voltage source inverters (VSI). Voltage source inverters produce square wave output. The harmonic content in the output voltage is approximately 50%. Additional filter circuits are used to filter out these harmonic components in the inverter output. Heavy filtering is essential to ensure a good quality output. The RMS value of output voltage obtained is always less than the input DC voltage in case of a VSI, hence it is termed as a buck inverter. Also, shoot through problem present in the VSI make it essential to provide dead time in the inverter switching. Current source inverters (CSI) are the next type of inverters which will have an inductor in the input side to ensure the current delivered is of constant magnitude. These CSI will eliminate the shoot through problem with the help of the inductor present. The output current obtained is square wave shaped and the output voltage magnitude is more than the input voltage level. Thus the inverter can be treated as a boost inverter.

To eliminate the shoot through issue and to incorporate both buck and boost capability, Z source inverters are introduced. Z-source inverters (ZSI) will have an impedance network consisting of capacitors and inductors. The impedance network is utilized to eliminate the shoot through and also, this shoot through state is used for the boosting of the input voltage. Buck boost capability is there with the Z source inverters but with the expense of bulky impedance network .This will increase the size and cost of the inverter.

Multilevel inverters (MLI) are another type of inverters conceptualized to minimize the harmonics in the output without heavy filtering and also with reduced rate of change of voltage. The concept is to incorporate as many number of voltage levels as possible so that the output will appear to be a sinusoid. In conventional VSI topologies the output voltage level is two. In MLI, the voltage level increases with increase in circuit complexity. As the level increases the transition from one voltage to other becomes very smooth and the output will be almost sinusoidal in nature. In this process, either number of switches, number of passive elements or the number of sources needs to be increased.

This will eventually increase the size and cost of the inverter. Also, the control will become complicated and thus implementation may require sophisticated controllers.

Mainly three types of multilevel inverters are available. Diode clamped MLI, Flying capacitor MLI and Cascaded H Bridge MLI. Each topology has its own advantages and disadvantages. The main constraint here with MLI is the size, cost and complexity of control circuit against an attempt to achieve pure sinusoidal output. Quality output without much complexity in circuit and control is the need of the hour in which more precise works are being undergone these days. The number of switches should be as minimal as possible without compromising the quality of output. Heavy filtering circuits as in the case of VSI also should be eliminated since that will further increase the size. Least harmonics possible should be the major objective to meet.

In this direction a new inverter topology termed Infinite Level Inverter topology is being introduced. The topology will ensure good quality output, minimum number of switches and high DC bus utilization in the three phase configuration without additional filter circuits. Unlike the conventional MLI topologies the voltage level is determined on the basis of switching frequency. Duty ratio is controlled to achieve infinite levels in the output voltage.

A conventional infinite level inverter comprises of a front end buck converter followed by an H bridge inverter. The buck circuit is sine modulated to produce fully rectified sinusoidal wave which will be unfolded in the next stage to produce near sinusoidal output. The need for five active switches and a passive switch is a drawback of the circuit. Also, there are unfolding ripples in the output waveform. Further reduction in the number of switches without reducing the quality and with the same conceptual grounds is the challenge which is addressed in this thesis.

In this work, a novel four switch infinite level inverter (FSILI) is proposed after the detailed investigation of the conventional ILI topology. The steady state analysis, design, simulation and implementation of the proposed FSILI are detailed in this thesis. Grid tied operation and its power control, three phase topology with maximum DC bus utilization and drive operation of the proposed inverter are simulated and analyzed.

1.1. Motivation of the Research

Multilevel Inverter was extensively used in the power sector because of different features they pose. The low switching stress and reduced harmonic content make them attractive for the power conversion applications. Also, the inclusions of more and more renewable sources in to the power sector necessitate the use of more efficient and reliable inverter systems. Also, the utility applications require clean and quality supply which will further foster the research thrust towards a better solution for the energy conversion applications. Many modifications were made in the conventional VSI and CSI topologies and impedance source inverters, dual buck inverters and multilevel inverters were introduced into the field owing to the demand from power market. Still, the active and passive component count, effective utilization of the available DC link, efficient power conversion with reduced THD are major challenges faced by the sector.

Also, the extracted power is to be effectively integrated to the utility grid for the use in an interconnected grid system. Efficient control algorithms along with low harmonic inverter output will make the extracted power more useful. There are challenges in the area of injection of extracted power into grid. The utility applications will require an inverter system which uses the available DC link in an effective manner. For drive applications and power quality improvement systems the output quality as well as the simplified structure is very important.

Motivated from the challenges, in this research, a novel infinite level inverter topology is proposed with minimal switches and simplified control logic. Its grid integration is achieved with a less complex control algorithm and is further modified into a three phase topology which is having high DC bus utilization.

1.2. Objectives of the Thesis

The objectives are

- To analyze the performance of conventional Infinite Level Inverters.
- To propose a Novel Four Switch Infinite level Inverter having low harmonic distortion and to perform its

- Steady state analysis and design.
- Simulation study and result analysis.
- Hardware Implementation and result validation.

➢ To introduce a Novel Three Phase Infinite level Inverter topology derived from proposed FSILI having minimum number of switches and

- To analyze the DC bus utilization under different modulation techniques
- To compare the performance of proposed Novel Three Phase ILI with the existing topologies

➢ To propose Grid Tied Four Switch Infinite Level Inverter topology with a modified current control technique capable of controlling active power injected onto grid.

1.3. Outline of the Thesis

The thesis is formatted as follows. In chapter 2 the literature review is described. The various RES, their extraction techniques, the existing inverter topologies and the modulation techniques, grid tied inverter topologies and their control methods, various three phase inverter topologies on the basis of DC bus utilization and different drive topologies are investigated in the literature. From the review the research problem is formulated.

In chapter 3, the conventional ILI topology with its three phase derivative is discussed. The concept, design and simulation are carried out for the conventional five switch ILI topology. In chapter 4, the novel FSILI topology is introduced. The steady state analysis, design of circuit components and simulation study both under open loop and closed loop condition are described in this chapter.

In chapter 5, the modified three phase ILI topology derived from the FSILI is detailed. With different modulation techniques the DC bus utilization of the proposed Three Phase ILI is analyzed. The simulation is carried out both under resistive load and motor load.

In chapter 6, the proposed grid tied FSILI is discussed. A current control algorithm and a new grid integration and control method are introduced. The power injection using the

proposed FSILI is analysed and which is simulated with different power levels for injection.

In chapter 7, the hardware implementation of the proposed FSILI is given. The experimental setup, the methodology and the results are described in this chapter.

Chapter 8 concludes the work and the various findings and projections of the work are detailed in this chapter. The future works which can be implemented to further enhance and enrich the topological derivations of the thesis are also pointed out in this chapter.

Chapter 2
Literature Review

2.1. Introduction

Quality electrical power is the driving force for most of the needs and requirements of modern world. Conversion of the available energy into the form suitable for conveyance and for the load requirements is very essential. In the history of modern engineering and in particular electrical engineering, efforts are made to ease the day to day life with the help of emerging technological developments. Inverters are such a move towards the sustainable development of mankind. Inverters are essential for power extraction from available renewable and alternative energy sources in this situation of depleting fossil fuels and conventional sources. Also, inverters are extensively used in various applications ranging from industrial drives to power conditioning of grid systems. A detailed review of different inverter topologies particular to renewable power extraction and various industrial applications is carried out. Apart from that, the works in the area of the grid integration of the extracted power is discussed here. In section 2.2., Different power extraction techniques came in the literature are reviewed. In 2.3., Inverter topologies used for renewable power extraction and which are used in industrial applications are detailed. In 2.4., a detailed study of different multilevel inverter topologies and different control algorithms available is carried out. In 2.5., the grid tied operation of inverters is described with the perspective view on the renewable power extraction.

2.2. Extraction of Energy from Renewable Sources

Energy is the vital element for the lively hood of human being in the world. The energy available in the planet is mostly from the fossil fuels which are depleting at a faster rate and now alternative solutions are being investigated. Nuclear energy is the one source of energy with large potentials. Many nuclear plants are being setup these days and large amount of power is being carried from these plants. The safety and security

issues are there with these nuclear plants and also the emission of radioactive materials as waste from these plants creates serious threat to the mankind and the living beings.

Renewable energy sources are one of the major alternatives for fossil fuels. Since they are clean, free from green house gas emission and are abundant in nature, these renewable sources are widely used for the power needs of the planet. Countries like Germany, USA, China and India have extensive projects for the extraction of renewable energy sources like solar and wind. In [1] detailed review of the energy utilization pattern in the modern era is depicted. Lata Tripathi et al (2016) [2] presented a review of renewable sector in India. As per [3], at present, 35.86% of the India's installed electricity generation capacity is from renewable energy sources. By 2030, it is expected to have 55% of total energy mix from renewable sources.

In [4] an overview of various renewable sources available for the possible extraction of power is detailed. Various sources like, solar photovoltaic, bio fuels, geo thermal, wind , hydro etc are listed with their share in the US energy sector, in this paper. B.sorenson (1991) [5] gave an early review on the trends in the renewable energy sector. Its future exploration rates are predicted with a detailed insight into the thrust areas. According to the research, the PV based DG systems will contribute to about 60% of the total energy generation within a matter of few years.

A detailed review of the various renewable sources with its increasing demand rate is depicted in [6].Hydro power is mostly used now a day, but the initial investment and the environmental impact create some serious concerns. Even then, it is forecasted that the capacity will grow from 42 GW to 115 GW in India by 2035. Carbon foot print of these energy sources is very less which makes them an attractive solution. But, it is expected that by 2070 there will be significant reduction in the hydro power potential in Europe and around the globe. Wind power has also drastically increased its share in the global energy market, rapidly increasing from 4.8MW in 1995 to more than 239GW in 2011. Off shore wind farms are making a way since it will eliminate the land requirement. Installation cost requirement is a big burden for wind power extraction. Serious issues are being identified and were investigated in order to have cost effective wind power

extraction systems which compromise the investment cost, frequency issues, power factor constraints and the government policy related to wind power generation.

Solar is an alternative source of energy [7] which is utilized highly over the last two decades. Solar market has increased its share from 9,564 MW in 2007 to 69,371 MW in2011. The solar Photo Voltaic systems can be installed in the dedicated solar plants, along with the hydro electric generation systems and in buildings. Solar electricity generation is considered to be having very less CO2 emission which is a favorable factor as far as the environmental pollution is concerned.

O. M. Babatunde et al. (2020) [8] gave a comprehensive review of various Hybrid Renewable Energy Systems, its need, different methods and the major focus areas of HRES will account for reduction in the CO_2 emission due to electricity production.

In [3] the renewable energy scenario in India is reviewed. Various economic, environmental and engineering aspects of renewable energy sources and its possible extraction are detailed in the paper. Fossil fuels are depleting in a very fast rate so that it is very essential for the country to look into available renewable sources. Solar, Wind, geothermal etc. are quite under exploited in India and can be used to meet the rising demand. Steps were taken by the government to enhance the use of more renewable sources and many new solar plants were commissioned. Wind power program and solar energy mission are implemented by government of India to foster the renewable sector. It is expected in India that among the total power generation the contribution from renewable alone can be of the extent of 60,000MW in the year 2031–2032.

Contributions of new and renewable sources are inevitable as seen from the aforementioned discussion. The most important aspect in the renewable energy extraction is making them available in the form of electrical energy. Methods for extraction of renewable energy are much discussed topic these days. Blaabjerg, F (2004) and Shahbazi et al. (2017) [9]-[10] gave a review of various power electronic interfaces used in the renewable power extraction systems. As Distributed Generation is being used to meet the increasing power demand, the integration of the individual sources into the grid is of prime importance. Authors explained the new trends in the power electronic interface

design which is very essential for these renewable system integration. Various converter topologies used in PV and wind energy conversion systems are detailed with their pros and cons given. The recent development in the PV system manufacturing and the advancements in the material science and the semiconductor technology greatly enhanced the market share of solar PV based renewable energy systems.

2.3. Inverter Topologies

Power conversion using power electronic converters is based on two basic and popular converter topologies: voltage-source and current-source converters. A voltage-source converter is fed from a constant voltage source that is generally smoothed through capacitors and a current source converter is fed from a constant current source that is generally supported by an inductor [11]-[14]. Each main switch used in VSI has to be able to convey bidirectional current and obstruct unidirectional voltage, thus the anti-parallel combination of a switch and diode is normally used. Figure 2.1 shows the circuit diagram of a three phase voltage source inverter. For a current source inverter shown in Figure 2.2., a reverse obstructing device or the series combination of a switch and diode is used as the main switch and it has to obstruct bidirectional voltage and only convey unidirectional current. There are certain short comings for these basic topologies which are listed below.

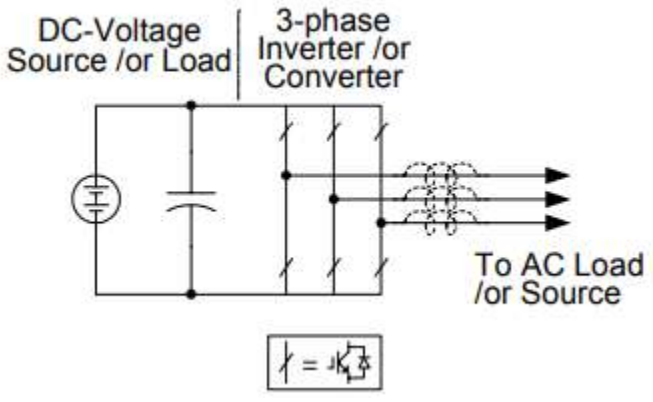

Figure.2.1. Three phase voltage source inverter

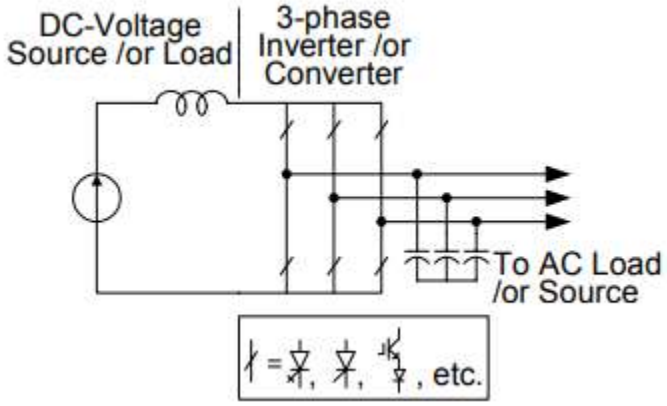

Figure.2.2. Three phase current source inverter.

1) VSI and CSI are either a boost or a buck converter and cannot be a buck-boost converter. That is, they are limited to low voltage, low speed and high voltage, high speed applications respectively.

2) The VSI is a buck inverter where the peak value of AC output voltage is less than the DC input voltage. CSI is a boost inverter where the peak value of AC output voltage is greater than the input DC voltage feeding the inductor. For applications exceeding the available voltage range, an additional boost (or buck) DC-DC converter is needed. This increases the cost and decreases the efficiency.

3) Their main circuits cannot be interchanged. In other words, neither the voltage source converter main circuit can be used for the current source inverter, or vice versa.

4) They are vulnerable to EMI noise in terms of reliability.

5) For a VSI, the upper and lower switches cannot be on simultaneously, which may cause a short circuit. On the other hand, for a CSI one of the upper switches and one of the lower switches have to be on to provide a path for the continuous input current.

The VSI/CSI requires dead time / overlap time to provide safe commutation which causes waveform distortion.

6) In a CSI, switch implementation requires diodes in series with the switches, which prevents the use of low cost switches which come with anti-parallel diodes implementation, as is usually it is manufactured.

F.Z. Peng (2003) [15] introduced a new inverter topology named Z-source inverter. Unlike conventional VSI or CSI inverters which have buck nature and boost nature in the input to output voltage level, Z-source inverter is capable of giving both buck and boost outputs. Figure.2.3. shows the circuit diagram of a Z-source inverter. The impedance network consisting of two inductors and capacitors resembles the Z shape and hence the name Z-source inverter.

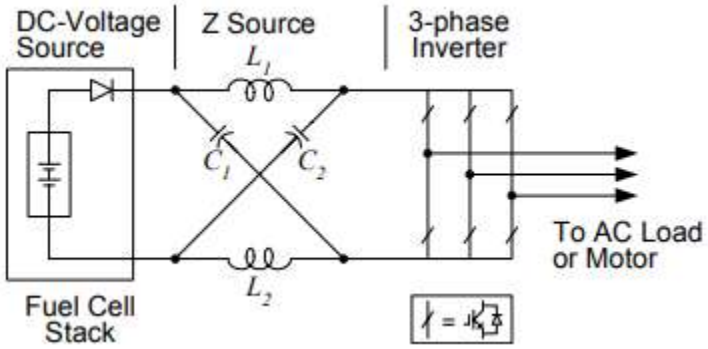

Figure.2.3.Z source inverter

B. Farhangi et al. (2006) [16] gave a detailing regarding the comparison of the Z-source inverter with the conventional inverters used for PV applications. Both buck and boost capability is the main attractive feature of impedance source inverters. The productivity of Z-source inverters came to be in the lower side when it is applied with large load where as the conventional inverters operated satisfactorily. When applied with renewable sources the voltage from PV, Fuel Cell etc will be fluctuating in nature requiring an additional boost stage in the front end in the case of voltage source inverters. Z-source as well as CSI does not require the same.

(M. Shen et al. 2007) [17] presented the operational concept of Z-source inverter. The different modes in the operation of Z source inverter is explained in this paper. Modes include shoot through and non shoot through modes. The shoot through operation, which is not permitted in VSIs are the major reason for the boosting obtained. The energy is

being stored in the impedance network during shoot through mode and will be transferred to load in the non shoot through mode.

Faruqui (2019) [18] did a comparative analysis of Z-source inverter with conventional inverters on the basis of number of components, circuit and control complexity, switching stress and THD. The effectiveness of Z-source inverters in the renewable energy application is also investigated.

The conventional Z-source inverter (ZSI) obtains high gain because of the uniqueness of its topology. In this inverter the duty cycle influences the voltage gain and so does modulation ratio. Modifications are made in the conventional Z source inverter topology and different topologies where derived. The bulky impedance network is replaced with an active switch and a single inductor along with the capacitor in the switched inductor Z-source inverter [19]. Quasi-Z source inverter [20] is another derived topology from the conventional impedance source inverter. Here many of the drawbacks of conventional ZSI are rectified. The input current burden in current fed ZSI is eliminated and also, the circuit complexity and control complexity are reduced. Trans Z-source inverter [21] is another modification in the ZSI in which inductor is replaced with a high frequency transformer. A transformer and a capacitor will be there at the front end and the inverter configuration is same as that of ZSI. It has all the features of ZSI at the same time have some distinctive features compared with conventional ZSI.

In the dual buck inverter configuration [22], the dynamic performance as well as the static performance is good. However, the inverter has poor utilization factor and increased volume because it requires two separate inductors and also needs to be fed using two separate voltage sources both of which should be independent of the other. The voltage gain of this topology is also less. The inverter in [23] has a dual Cuk configuration, one inverting and the other non-inverting. This inverter employs six power switches out of which four are high frequency switches. It steps up or steps down the input voltage because of its inherent features. However, maintaining high efficiency is difficult and the inverter configuration is complex as well.

Manoj Kumar et al. (2014) [24] reviewed the power electronic interface used in the hybrid renewable energy systems. The solar and wind energy systems require different power electronic interface. In wind energy conversion systems, the variable frequency AC is being converted into grid frequency AC. Where as in PV systems the DC power obtained from PV is to be converted into AC with the help of DC-AC converters (Inverters).

In [10], [25] the different power electronic interfaces used for power extraction purpose are discussed. Sources with different nature require different types of converters. PV based systems may have power converters connected either in series or parallel. Centralized, string configuration and AC module method are the different types of inverter configuration used in PV systems. If the voltage at the PV side is low, may need to have a boosting circuit at the front end. A line frequency transformer will also be used along with this boosting circuit. Line frequency transformers are bulky, less efficient and expensive.

Multi stage converter systems [26] employ a DC-DC converter which will also perform the maximum power point tracking (MPPT). A high frequency transformer in the DC supply side can provide galvanic isolation and boosting. This stage will be followed by an inverter either single phase or three phase according to the power level.

Hence there is a requirement of transformerless single stage inverter configurations [27]-[28] a few of which have been investigated in the recent past. Debnath et al. (2016) in [29] proposes a new buck boost integrated full bridge inverter topology which incorporate a buck boost converter onto inverter to achieve a single stage operation while extracting power from solar PV systems. The main advantage is the gain obtained along with the reduction in power loss. The circuit makes use of body diodes for the completion of current path and it requires a DC side capacitor and inductor apart from the filter inductor and capacitor present in the AC output side. Even though buck boost nature can be obtained across the capacitor, across the output terminal, the voltage obtained is boosted only.

Transformers less topologies have the advantage that both circuit complexity and control complexity can be eliminated. Multi stage topologies will have reduced overall efficiency due to losses in the individual stages. Some topologies use buck boost converters in place of boost converters. Multilevel inverters are another solution available to obtain a smooth and low harmonic output voltage with reduced switching stress.

Leakage current is prevailing in transformerless topologies due to the PV parasitic capacitance [30]. The common mode current due to this parasitic capacitance should be suppressed. Different topologies are in practice to eliminate this leakage current. By making the common mode voltage constant, the leakage current can be eliminated. This can be achieved by isolating PV from the AC side during the freewheeling cycle of the inverter.

H5 inverters [31]-[32] are introduced to suppress the leakage current in which an additional switch is provided in the DC side to provide the freewheeling path. In the case of a single phase H5 inverter, the upper switch of this full bridge inverter topology operates at grid frequency. However it has high switching losses and reduced efficiency. The H5 inverter is modified by adding two more switches in [33] in order to reduce the switching losses and to increase its efficiency. The paper explains a transformerless topology of renewable power extraction. Soft switching technique is used here for the reduction in switching loss. Also, isolation of the grid side from the PV side is achieved with the additional soft switching devices. Circuit with 7 switches and more number of capacitors and inductors makes the inverter circuit complex. Figure.2.4. Represent a H5 inverter used in PV systems.

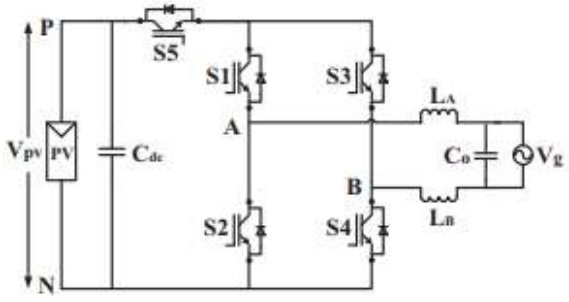

Figure.2.4. H5 inverter for PV system

High Efficient Reliable Inverter Concept (HERIC) [34] is another modified topology in which two switches are provided in the AC side to decouple the PV and the grid. Figure.2.5. depicts the HERIC topology.

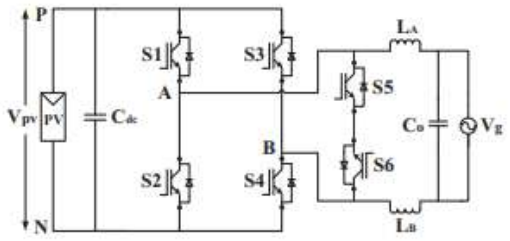

Figure.2.5. HERIC inverter for PV system

H6 inverter [34]-[35] is another topological change done for the leakage current suppression. This inverter is a zero state midpoint clamped topology. This topology can handle reactive power to an extent.

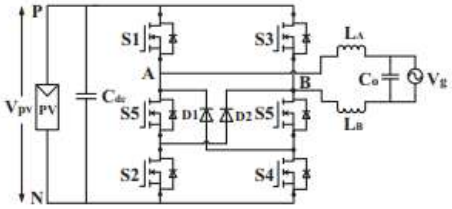

Figure.2.6. H6 inverter for PV system

H4, H5 and H6 inverters are compared in [36] and a seven switch step-up inverter is presented in [37]. [38] Gives a modified H6 inverter which has reactive power flow capacity and is highly efficient compared to previous topologies. From these topologies it can be concluded that all these configurations have large number of switches, and passive components and the driving circuit is also more complex.

H7 inverter developed by modification of H5 inverters is presented in [39] in which modified discontinuous pulse width modulation (MDPWM) [40] is used to develop control pulses. This is a complex method and hence not preferred. Boolean logic was used to implement another modulation technique [41] which is simple and does not require space vector modulation [42]. Other modulation techniques like unipolar and

bipolar methods are presented in [43]. All of these modulation techniques show that the type of modulation used affects the leakage current in the inverters.

Xue et al (2004) [44] gave a review of basic inverter topologies used in small distributed power generation systems. Distributed generators are increasing the share since the demand for electrical energy can't be met with conventional sources. Here in small DG systems, the inverter does the function of delivering power to AC loads and to integrate sources to AC grid. Broadly inverters employed for this function can be classified into isolated type and non isolated type inverters. Such inverters used should ensure minimal THD while converting fluctuating DC into AC. Based on the input to output voltage ratio, inverters can be buck, boost or buck boost in nature. A detailed review of different 4 switch and 6 switch topologies were made here. Each topology on the basis of pros and cons is detailed. The latest developments and future trends are discussed with an insight into research possibilities. In case of multi stage topologies overall conversion efficiency is very less and the power loss is more.

Commercially available configurations employ transformers for galvanic isolation between the inverter and AC grid side in order to prevent entry of DC currents to grid. Line frequency transformers will lead to a bulky conversion system whereas high frequency transformers lead to complex system. Efficiency of such inverters will also be less due to core losses. Hence, apart from being transformer less, the inverter configuration should be such that it should convert the input DC from sources like PV into AC voltage at the grid side [45]-[46].

2.4. Multilevel Inverter Topologies

The output of the two level conventional inverter is either +Vs or –Vs. The output is having high harmonic content which should be filtered out. High voltage and current stress is another issue faced by these conventional inverters. High frequency operation will reduce the harmonics but at the same time power loss will be increased limiting the operation to high power applications. Multi level inverters are introduced to solve the above issue with the help of a combination of switches and DC sources. With the recent advancements in the field of power electronics and its control, a new breed of power

electronic converters is being emerged , known as multilevel inverters [47] -[77]. The concept of MLI is extensively used in industries and many manufacturers have taken patents and it is emerging as a prominent choice in the industry for medium voltage applications including drives and power system compensators.

2.4.1. Concept of Multilevel Inverter

Conventional inverter produces only two levels in the output voltage and PWM is used to form the AC output waveform as shown in Figure 2.7. Even though the AC output waveform is produced it has high harmonic distortion and also, the voltage stress on the switch will be very high.

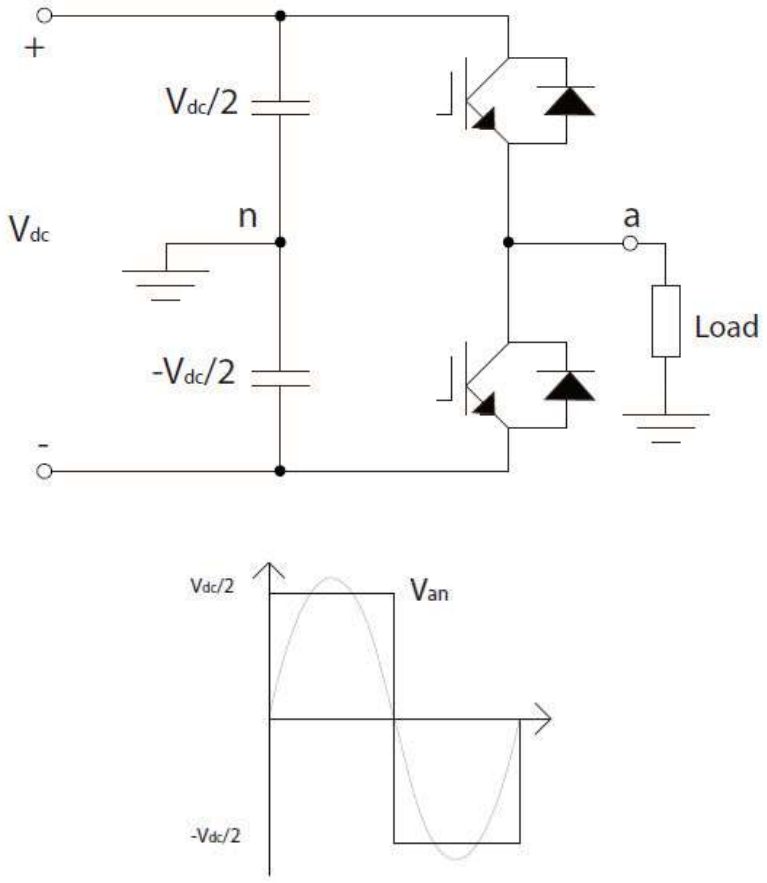

Figure 2.7 .One phase limb of a two-level inverter and a two-level waveform

In multilevel inverter more than two voltage levels are generated which approaches a pure sinusoidal output voltage wave form as the voltage level increases. A multilevel inverter generally can be said to have the capability to produce stepped waveform which has low voltage stress and low harmonic distortions. With increasing levels the circuit becomes more complex due to additional switches and elements and also, control will become more complicated. The generalized stepped waveform is shown in Figure 2.8.

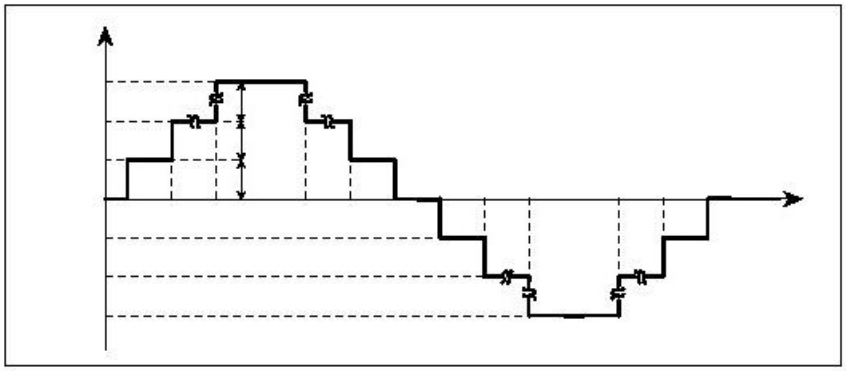

Figure.2.8. Generalized stepped waveform

Major classification of MLI is made based on the topological differences. They are

1) Diode clamped multilevel inverter.

2) Flying capacitor multilevel inverter.

3) Cascaded H-bridge inverter.

Some of the advantages of multilevel inverter over conventional two level inverter are listed below.

1) Reduced harmonic distortion and high power quality

2) Near sinusoidal output due to the multiple levels in the output voltage

3) Capability to operate both with fundamental frequency PWM and high frequency PWM modulation.

4) Minimal switching losses.

5) Low rate of change of voltage and thus nominal switching stress.

6) Common mode voltage is less which makes the converter suitable for drive applications.

The three basic topologies of multilevel inverter were discussed by [50] J. Rodriques, Jih Shing et al. Also the modulation schemes employed in the MLI like multilevel sinusoidal PWM, MLI, SHE and SVPWM. Also the major applications of the MLI topologies were explained.

The applications of the multi-level inverters were also discussed in this paper. MLI was first used in drive applications [48], [51]. Reactive power and harmonic compensation [52] is another area where MLIs are used. Area of Power system conditioning also make use of multi-level inverter. Reduction in cost, and in Electromagnetic Interference, with an increased efficiency compared with the conventional inverters make MLI a suitable option for power system applications. Cascaded MLIs are mainly employed in these applications. Vienna Rectifiers have now emerged as an application of multilevel topology. UPFC and STATCOM also make use of multilevel concept for a better performance.

J.S. Lai et al. in [47] , gave a survey of multilevel inverters in general and a detailed study of three basic topologies in multilevel inverters. Multilevel inverters produce more than two levels in the output voltage. As the number of levels increases, the output will become more sinusoidal and will be with fewer harmonics. Hence, filter with low rating is enough to get pure AC output.

2.4.2. Diode Clamped Multilevel Inverters

Nabae et al. (1981) proposed a neutral point clamped PWM inverter [53] which has less harmonic content compared to the conventional PWM inverters. A basic derivation of multilevel Inverter came from this work in which neutral point clamping with diode is used. Harmonics are less and torque pulsations are reduced for drive applications. Even though the number of switching devices is double that of conventional inverters, the output kilo Volt Ampere rating is increased two fold. Selective Harmonic

Elimination can be incorporated with this topology for harmonic reduction. The proposed topology with the help of more number of switches and diodes can be modified to obtain near sinusoid output with more number of levels.

Later the neutral clamped topology is extended to higher levels [54] and the topology is generalized as diode clamped multilevel inverter. For obtaining different voltage levels in the output clamping diodes are used here, hence the name diode clamped MLI. Figure.2.9. Shows the circuit diagram of a diode clamped MLI. In diode clamped MLI, Number of switches for m-level= 2(m-1), number of input voltage source= (m-1) and number of clamping diodes = (m-1)(m-2).

The features of DCMLI are the requirement of high voltage rating for the blocking diodes; device rating is not same, unbalance in capacitor voltage level etc.

The advantages of DCMLI include the possible elimination of filter capacitors at higher voltage levels, switching at fundamental frequency increases the efficiency and the possibility to control the reactive power.

The major disadvantages are increase in the number of clamping diodes as the level increases making the inverter more complex and bulky. Also, it is very hard to control the real power flow control in individual inverters. This topology requires high speed clamping diodes that must be able to carry full load current and are subject to severe reverse recovery stress. Although measures to alleviate this problem can be applied, this remains a serious consideration.

For topologies with more than three levels the clamping diodes are subject to increased voltage stress equal to $Vpn\,{}^{m-1}/_{m}$ .Therefore, series connection of diodes might be required.

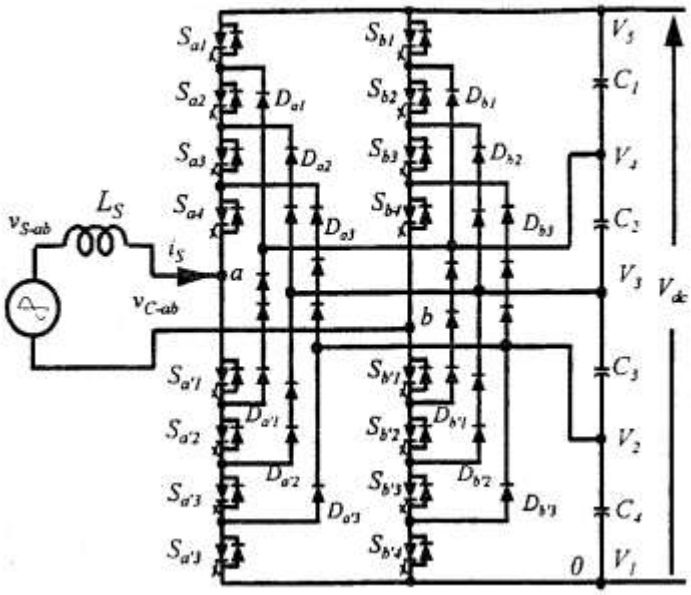

Figure.2.9 Diode clamped multilevel inverter.

2.4.3. Flying Capacitor Multilevel Inverters

J.S. Lai et al. [47], further explains flying capacitor multilevel inverters. Flying capacitor MLIs [55] are very similar to diode clamped MLIs. Here the clamping devices are capacitors and the synthesis of voltage level has more flexibility than DCMLI. As the capacitor used here float with respect to the earth potential, the name flying capacitor is given. The need for balancing the voltages at the capacitors and the requirement for more number of storage capacitors is a major challenge faced in a FCMLI. Thus the packaging becomes difficult and the size of the inverter is very high for high power ratings. The inverter control comes to be very complex and for real power control switching frequency and switching loss will be more. Figure 2.10 shows the circuit diagram of a flying capacitor MLI.

For a m-level MLI, cascaded MLI will have 2(m-1) switches, (m-1) DC link capacitors and ((m-1)(m-2))/2 auxiliary capacitors.

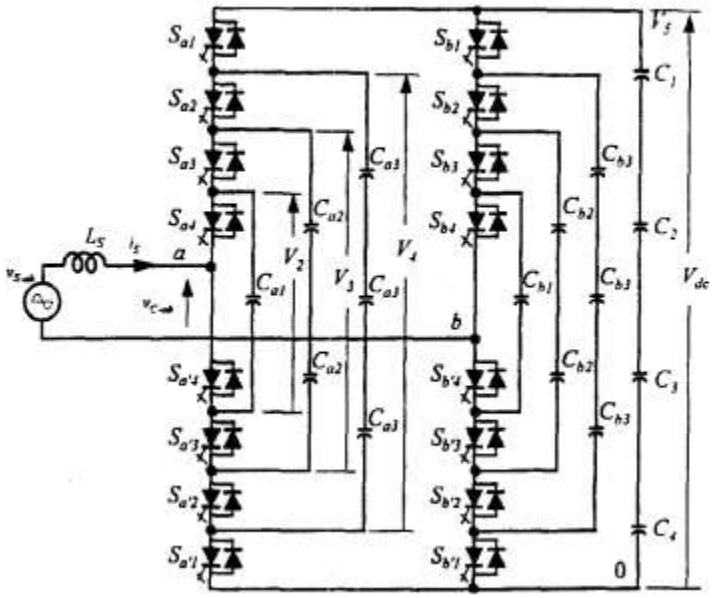

Figure.2.10. Flying capacitor multilevel inverter

2.4.4. Cascaded H Bridge multilevel Inverters

Cascaded H bridge multilevel inverters are another class of multilevel inverters [56] which uses separate dc sources. Additional clamping diodes or clamping capacitors is eliminated here. Figure.2.11 represents the basic circuit configuration of five-level cascaded H-bridge multilevel inverter (CHBMLI) topology. Output voltage is obtained by summing up the individual module voltages. The resultant output ac voltage magnitude fluctuates from $-2V_{dc}$ to $+2V_{dc}$ through $-V_{dc}$, 0 and $+V_{dc}$ with five-levels. The obtained output voltage waveform is close to a sinusoid without any filtering. By increasing number of input sources we can obtain a better quality output. In three phase CHBMLI topology, three individual CHBMLI are connected either in star or delta .Output voltage level in CHBMLI can be given as 2n+1, where 'n' is the number of input sources. CHBMLI requires lesser no of switches than diode clamped multilevel inverter.

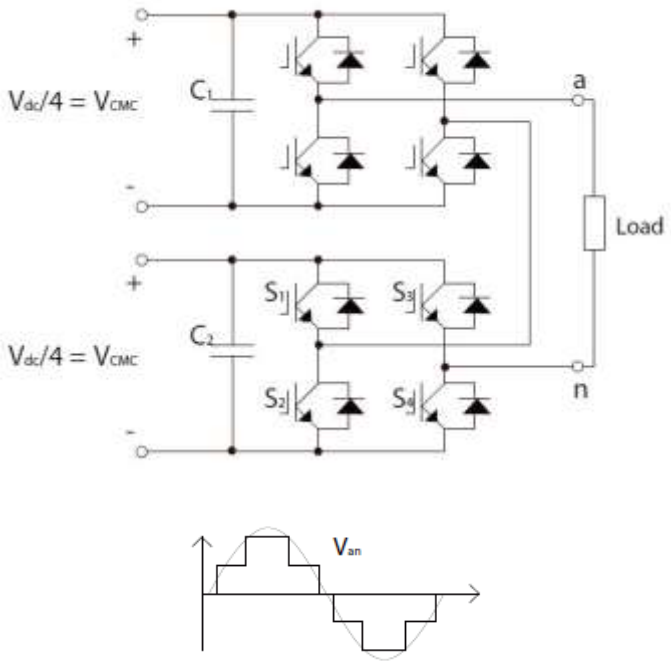

Figure.2.11.Single-phase structure of a 5 level multilevel cascaded H-bridge inverter

The main attractive feature CHBMLI is modularity of its structure which enables easy maintenance and also it adds to the redundancy of the system. The multilevel inverter using cascaded-inverter with separate DC source synthesizes a desired voltage from several independent sources of dc voltages, which may be obtained from batteries, fuel cells, or solar cells. This configuration recently becomes very popular in ac power supply and adjustable speed drive applications

Malinowski et al. (2010) [57] gave a review on different cascaded multilevel inverters. Cascaded MLI uses series connected single phase inverters. Among the three basic MLI topologies, CHBMLI reached highest power level. Modular nature makes it more faults tolerant. The main short coming of CHBMLI is the requirement for isolated DC source. The value of DC link voltage can be same or different depending upon the topology used, most common being CHBMLI with same DC link voltage. When they are used in reactive power compensation applications, the DC link can be with a capacitor.

The paper reviews various types of cascaded MLI topologies including symmetrical and asymmetrical configurations. Regenerative topologies discussed by H. Liu et al. (2008)

[58] are a later development CHBMLI which are commonly used in drive applications. The front end rectifier is modified as controlled rectifier for the purpose. Bidirectional capability will be enhanced by the regenerative property of the inverter.

Vahidi H.et al. (2019) [59] discussed the pros and cons of multi DC source inverters. In CHBMLI multiple DC sources are used. Modularity and identical voltage rating of switch are major advantages of CHBMLI in case if symmetrical type is employed. In case if the asymmetrical type is used, the switch rating cannot be identical. Since the number of sources is more, size is more and cost is also high in CHBMLI.

2.4.5. Comparison of Multilevel Inverters

In high power system, the multilevel inverters can appropriately replace the exits system that uses traditional multi-pulse converters without the need for transformers. All three multilevel inverters can be used in reactive power compensation without having the voltage unbalance problem. Table 1 compares the power component requirements per phase leg among the three multilevel voltage source inverter mentioned below. It shows that the number of main switches and main diodes, needed by the inverters to achieve the same number of voltage levels. Clamping diodes were not needed in flying-capacitor and cascaded-inverter configuration, while balancing capacitors were not needed in diode clamp and cascaded-inverter configuration. Implicitly, the multilevel converter using cascaded-inverters requires the least number of components.

Table 2.1: Comparison of three multilevel inverter topologies

Inverter configuration	**Diode clamped**	**Flying capacitor**	**Cascaded H bridge**
Main switching devices	2 (m–1)	2 (m–1)	2 (m–1)
Main diodes	2 (m–1)	2 (m–1)	2 (m–1)
Clamping diodes	(m–1) (m–2)	0	0
DC bus capacitors	(m-1)	(m-1)	(m-1)/2
Balancing Capacitors	0	(m – 1) (m –2)/2	0

2.4.6. Control Methods of Multilevel Inverters

Based on the control and modulation strategies MLI [50] can be classified into fundamental switching frequency and high switching frequency PWM types [60], [61]. Figure 2.12.shows the different methods available under each category. Fundamental frequency switching strategies are again divided into space vector control and selective harmonic elimination method. Space vector modulation and sinusoidal pulse width modulation control are the modulation strategies employed in high frequency PWM method. The low frequency switching methods will have one or two commutations of a switch in one cycle. Whereas, the high frequency switching strategies have more commutation of switch in a cycle itself. Sinusoidal PWM is the classical method employed for harmonic reduction. SVPWM technique [60], [62] can be used in three phase inverters to maximize the harmonic reduction and output voltage amplitude. Sine PWM technique is again classified into phase shifted carrier and level shifted carrier techniques [63], [64], [65].

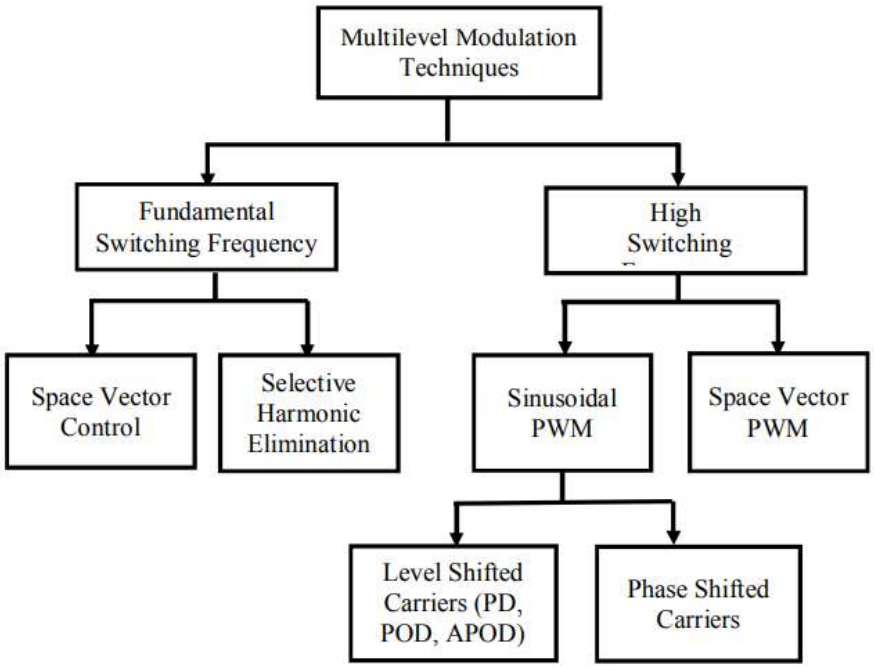

Figure 2.12 Classification of MLI modulation techniques.

The main aim of any modulation method is to obtain the desired output from the inverter. Also, the modulation techniques employed in MLI will reduce the harmonics; reduce the switching stress by properly operating the switches with the appropriate modulation scheme. Lower switching frequency methods will have lower switching loss and better efficiency. High frequency method will have reduced harmonics compared with the fundamental frequency methods. High frequency methods require complex drive circuits where as the low switching frequency modulation techniques need simpler driver circuits.

The conventional space vector PWM techniques can be easily extended to MLI topologies with an increase in the number of switching vectors as the output voltage level increases [65]. As the output level increases, the switch redundancy and the complexity in selecting switching state increases drastically.

Selective Harmonic Elimination (SHE) [66], [67] is a low frequency modulation strategy which will eliminate a desired harmonic component from the output. The switching angles are found out for eliminating some of the dominant harmonic terms. The switching angles are found out by solving transcendental equations obtained. The equations can be solved by numerical methods like Newton Raphson method, Gauss Seidel method etc. A narrow range of modulation technique is the major drawback of the method.

Sinusoidal PWM techniques are one of the common modulation method used in the 2-level inverters. Sine PWM method will eliminate harmonics considerably and filter size can be drastically reduced. When extended to multi level inverters [64], [65], [69] there are two major divisions in the sine PWM modulation techniques. 1) Phase shifted multi carrier method and 2) Level shifted multi carrier method.

Phase shifted carrier method [69] will have high frequency carrier waves shifted from one another. This method is commonly used in CHBMLI and FCMLI topologies. Figure 2.13 shows the pulse generation logic using this method.

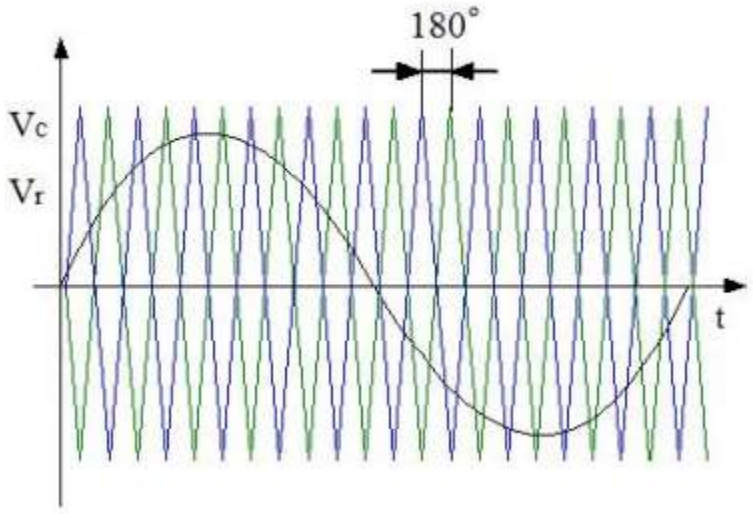

Figure.2.13 Phase shifted multicarrier modulation technique.

Level shifted multi carrier methods [65] include Phase Disposition (PD), Phase Opposite Disposition (POD) and Alternative Phase Opposite Disposition (APOD). Figure.2.14 shows the three different PWM methods coming under the level shifted modulation. In IPD,

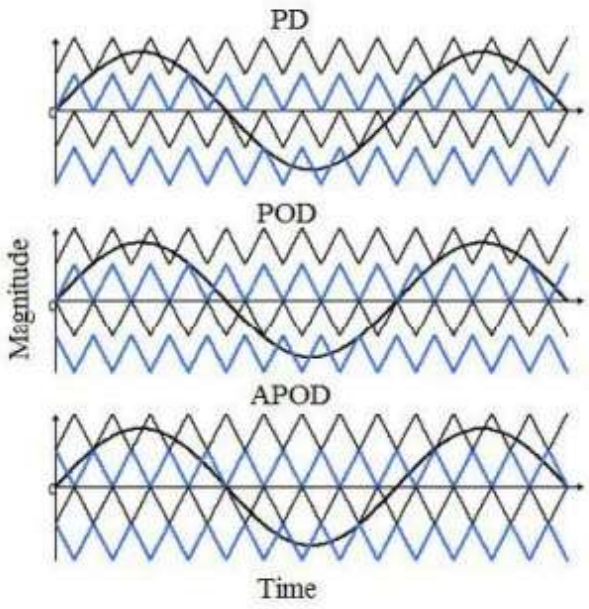

Figure.2.14 Level shifted multicarrier modulation technique

2.4.7. Other Multilevel Inverter Topologies

Babaei et al. (2014) [70] gives the details of two advanced MLI topologies with series and parallel connection of DC sources is given. The output voltage level is increased with a minimum blocking voltage for individual switches. Optimal structure is obtained so as to get maximum voltage level. For a seven level output only 4 switches required.. Compared to conventional topologies, this topology will reduce size, cost and losses. Number of DC sources used in this topology is more in comparison with similar topologies.

A comparison of different modulation methods for MLI was carried out in [71]. The difference in the operation when sine PWM control is applied with different carrier signals and modulation methods is studied. Both line and phase voltages are analyzed for the distortion present with different methods of modulation.

Babaei et al. (2015) [72] proposed a single -phase cascaded multilevel inverter topology with series connection of the basic H-bridge units. 9 distinct algorithms are derived from the basic unit with different combinational connections. Best possible algorithm among the 9 topologies found by analyzing the topologies on the basis of number of switches, number of sources and its nature. The best topology obtained is then compared with conventional topologies to understand the merits. Depending on the way in which basic units are connected, different equations are obtained for the number of levels in the output voltage.

P. A. Salodkar et al. (2017) [73] discussed control of a single phase seven level inverter topology reduced components using proportional integration controller. The pulse width modulation is employed to generate gating signals for power switches. This topology can be implemented for three phase application. The circuit consists of two parts 'Level generator' and Polarity generator'. The switches in level generation part operate at higher switching frequency whereas switches in polarity generation operate at power frequency.

Arpan Hota et al. in [74] gave the details of an optimized, 3-ϕ, multilevel (MLI) inverter topology derived by cascading the level generation part with the phase sequence

generation part. Further, it can be operated at any required level depending upon the configuration of the level generation part. Also, each dc voltage source in the presented MLI topology is equally shared by all the phases. Thus, any chance of inter-phase asymmetry is avoided.

S. Raghu Raman et al.(2017) [75] A switched-capacitor multilevel inverter for high frequency AC power distribution systems that produces a staircase waveform with higher number of output levels employing fewer components compared to several existing switched capacitor multilevel inverters is presented. The inverter inherently solves the problem of capacitor voltage balancing as each capacitor is charged to the value equal to one of input voltage every cycle**.**

Hemant Gupta et al. (2016) [76] Cascade multilevel inverter is the best suitable topology among the other multilevel inverter topologies in STATCOM application due to its distinguished featuring like modularity in structure and feasibility in control design in terms of less switching losses and better ac output waveform quality. In this paper special attention is dedicated to increase the reliability of the system by presenting the general control design for the system by which dc link voltage balancing and reactive power compensation can be carried out by using the nine-level cascade multilevel inverter as STATCOM.

Siddique (2019) [77] proposed a new multilevel Inverter topology which produces staircase output voltage with reduced switch count. In the first proposed topology, there are 15 levels in the output and which is obtained with the use of 3 DC sources and 10 switching devices. The second topology has 25 output voltage levels obtained by employing 4 DC sources and 12 switches. Apart from the reduction in switch count, the stress on the switching devices are also very less.

2.5. Control and Grid Integration of Inverters

Distributed generation is evolving as the major contributor towards the power requirement of the world. Both islanding mode of operation and grid connected mode of operation are possible for DG systems. Wind, Solar PV, Fuel Cells etc are the key

sources which are used in DG systems. In which especially integration of PV based systems are showing exponential growth. In [78] an overview of control and grid synchronization of distributed generated systems is done. The integration of these DG systems may cause to have stability issues in the grid and also will deteriorate the quality of the grid supply. It is of prime importance that the power which is to be integrated to the grid should be controlled adequately to eliminate the stability issues. Also, the current being injected to the grid must be with good quality. Also, the efficiency of PV systems is very low indicating the need for maximum power point tracking. So, it can be concluded that, the DGS should have an input side controller and a grid side controller. While the input side controller ensures the MPPT and input side protection, the grid side controller enables proper synchronization of the injected supply with grid, control of active power supplied to the grid, control of reactive power transferred between grid and DGS, Control of DC link voltage and ensure the quality of power being injected.

Various grid control and synchronization method of distributed power generation systems are also discussed in [78]. The grid side control is achieved in different structures. It may have an inner current loop and an outer voltage loop. Reference [79] Explains different topologies of grid control with inner current loop and outer voltage loop which are capable of operation under faulty conditions also. Indirect current control is achieved with an inner power loop and an outer voltage loop in [80]. Another implementation is with an outer power loop and inner current loop [81]. Here the reference current is obtained from the power reference. A fuel cell based DG system in which fuel cell power is taken as the variable of control and compared with the reference power level to obtain the current reference.

The control implementation is done either in the synchronous reference frame, stationary reference frame or in the natural reference frame. In synchronous reference frame [82], by doing Parks transformation, the three phase quantities are converted into DC quantities. PI controller [83] is used here since DC is the control variable. In stationary reference frame, here *abc* quantities are converted into $\alpha\beta$ reference frame, in which the quantities are sinusoidal. So, PI controller will not be able to minimize the steady state error. Proportional Resonant Controller [84], [85] (PR controller) is used here. PR

controller has the capability to achieve very high gain around the resonant frequency enabling the elimination of steady state error. In natural reference frame also it is possible to control the power injected into grid. Here PI controller with certain modifications, PR controller, hysteresis current controller or dead beat controller can be used. Hysteresis controllers [86] are very simple and can be implemented in single phase or three phase systems. An adaptive band hysteresis controller is used to make the switching frequency constant.

For proper injection of current in phase with the grid voltage, the phase of grid voltage should be known. One method is to do grid voltage filtering to obtain the phase angle. Transformation angle detection (TAD) [87] filters are used here. Another commonly accepted method is to use Phase Locked Loop (PLL).

Phase Locked Loop (PLL) [88], [89] are used in communication systems, servo systems and also in grid control applications. It can be implemented with analog, digital or hybrid ICs. PLL is one of the commonly accepted methods to find the grid voltage phase angle and thus ensuring proper synchronization of injected power. In [90] a hysteresis control method which produces the current reference without employing PLL is explained. In [91] a novel AC current sensorless hysteresis control for grid tied operation is presented. More accurate switching is achieved here but the control became very complex.

Power electronic converters are the essential elements of the grid integration of RES. In [9] different power electronic converters used in RES are reviewed. From the review of different inverters on the basis of output quality, control and circuit complexity, for renewable power extraction, many solutions emerged like z-source inverters, transformerless inverters with leakage current suppression and multilevel inverters. Multilevel inverters will reduce the switching stress, make the output distortion free without extensive filtering and are some of them modularity in their construction. Also, the different available modulation techniques indicate the feasibility of the MLI to be used in industrial applications also. In [92] a combination of cascaded H bridge MLI and a quazi Z-source inverter is proposed which is capable of eliminating grid unbalance issues. Against the various advantages of multilevel inverters the major drawback of MLI is the increase in the component count as the number of output voltage levels increases.

Some of the topologies need more diodes and capacitors whereas the some others may require more number of DC sources. Infinite level inverters are a new class of inverters introduced to overcome most of these drawbacks. Here, unlike the conventional MLI the output voltage level is determined by the switching frequency. There is no need for additional filter circuit and only one switch need to be operated at high frequency. In this work, an improved infinite level inverter is investigated.

2.6. Summary

Various renewable energy sources available to replace the existing depleting sources are reviewed with the focus on extraction of power. The role of inverters in the renewable power extraction is depicted with a detailed survey. For the drive applications and other industrial and house hold applications the different topologies of inverters used in the market are studied. VSI, CSI, ZSI etc are extensively used but due to several limitations they have, more investigation is being done in the area of multilevel inverters. Multilevel inverters are viable solutions for the efficient power conversion of available DC into AC. Different multilevel topologies are introduced and the modulation techniques employed for harmonic elimination are also discussed. The latest developments in the MLI focus on the development of topologies which can be used in the renewable power extraction having improved output quality. The grid integration of inverters is also very important since the extracted power needs to be injected in to utility grid. Review of various grid control methods are detailed indicating their pros and cons. The major challenges in the multilevel inverters are found to be the increased number of components, either switches or the capacitors which adds to the complexity of the circuit. The research is focused on the development of new topology of inverter having maximum levels in the output with reduction in the component count. Investigation of infinite level inverters and development of a novel infinite level inverter topology is indented in this research. From the review carried out on the three phase inverter topologies, the DC bus utilization is very prominent parameter as far as the medium and low voltage systems are concerned. Further, a three phase extension of the proposed ILI topology is another area where the research moves in. The grid integration of the

developed inverter with a modified grid control algorithm will be done to understand the feasibility of the inverter in the grid tied operation.

Chapter 3

Conventional Infinite Level Inverter Topology

3.1. Introduction

Conventional multilevel inverters are capable of producing output voltage with minimal distortion with a nominal switching stress. But, the available MLI topologies have the limitation that the component count increases drastically as the level of voltage increases. The overall efficiency may come down, the inverter will become bulky and the cost will also get increased. In this chapter concept of infinite level inverter (ILI) is explained. The output voltage level is a function of switching frequency and the voltage will follow the duty ratio variation to achieve maximum possible levels. Single phase ILI topology is explained and the derived three phase ILI topology [93]-[95] which is having better DC bus utilization in comparison with existing topologies and control is also analyzed in detail. Simulation of both single phase and three phase topologies are done and investigation on the quality of output obtained and FFT analysis are also performed.

In section.3.2.the concept of infinite level inverter is explained with the explanation of various modes of operation. Section.3.3. gives the details of three phase infinite level inverter which is having many attractive features. The simulation study carried out for both single phase and three phase ILI is explained in section 3.4. The features of ILI are listed in section 3.5. Section.3.6. gives the limitations of conventional ILI topology. Section.3.7. gives the summary of the chapter.

3.2. Concept of Infinite Level Inverters

Infinite level inverter (ILI) topology is a solution for some of the problems encountered in the conventional inverter topologies. ILI has a front end buck converter followed by an H Bridge inverter. The buck converter will operate at high

frequency that too with sine PWM switching. The buck converter output will be rectified sine output voltage. The output of the inverter will be purely sinusoidal unlike normal inverters. Also, the shoot through problems are absent in this topology. Figure.3.1. shows the circuit diagram of the Infinite Level Inverter topology. No additional filter circuit is required in this topology since the output obtained is with very less harmonic distortions.

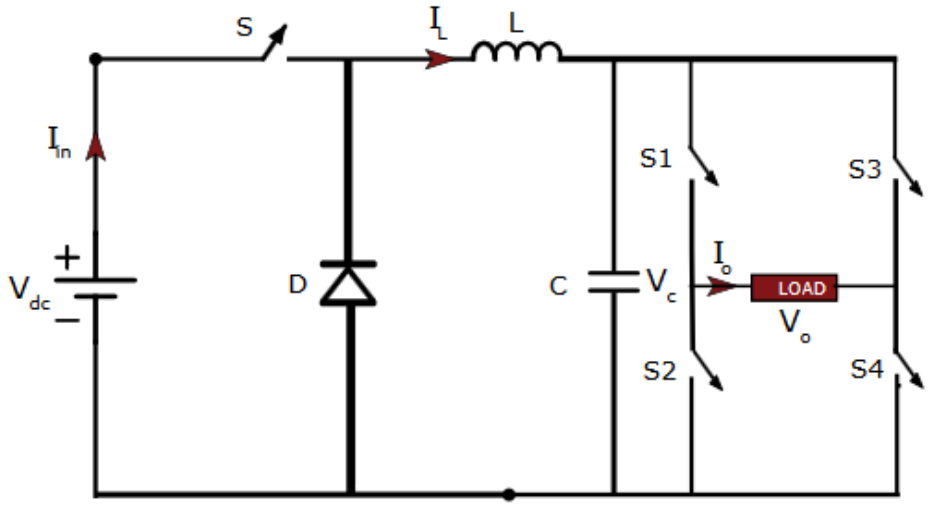

Figure.3.1. Circuit Diagram if Single phase ILI

3.2.1. Principle of Operation of Infinite Level Inverter

$$For\ a\ buck\ converter\ we\ have, v_o = dV_{dc} \tag{3.1}$$

Keeping the input voltage constant, the duty ratio d is increased in steps as per the switching frequency in the form of a fully rectified sine wave. This can be given as

$$d = D|sin\omega t| \tag{3.2}$$

Therefore we can write,

$$v_o = V_{dc}D|sin\omega t| \text{ for } 0 < \omega t < 2\pi \tag{3.3}$$

The output obtained for the front end buck converter is fully rectified sine wave which will be unfolded using the H bridge inverter in the fundamental frequency. This will result in a sinusoidal output voltage and current when the buck converter is operated at high frequency. In conventional multilevel inverters to make the output distortion free, the number of output voltage levels is increased. For increasing the number of voltage levels, MLI requires more number of switching devices or sources. The number of capacitors may also be increased in some topologies. Here, the output voltage level is a function of carrier frequency. As the switching frequency increases, the output voltage level increases and it will be very close to a sinusoidal waveform. Thus, the harmonics of the infinite level inverter is considerably low. In the three phase topology, the DC bus utilization is very high which will reduce the voltage stress on the switches and other passive elements.

3.2.2. Modes of operation of single phase ILI

Infinite level inverter has four separate modes of operation. Two modes each for positive and negative half cycles. In modes I and III, the high frequency switch S will be ON. In mode II and IV, switch S will be in OFF condition. The H-bridge inverter switches will be operated at fundamental frequency. In the positive half cycle, S_1 and S_4 will be turned on and S_2 and S_3 will be unexcited. In negative half cycle, switches S_2 and S_3 will the operating switches. The assumptions made while analyzing the operating modes of the inverter are

1) For a particular switching period, duty ratio and output voltage remains constant.
2) Switching frequency is very much greater than the output ac voltage frequency.

The capacitor gets charged and discharged while the high frequency switch operates and a positive fully rectified voltage is maintained across the capacitor.

Mode I

In mode I, the high frequency switch in the front end will be in ON state. The inductor L will be charging. The diode D will be reverse biased. The switches S_1 and S_4 of the H-bridge inverter will give a path for positive current. The load voltage will be positive in this mode. Figure 3.2 shows the current path in mode I.

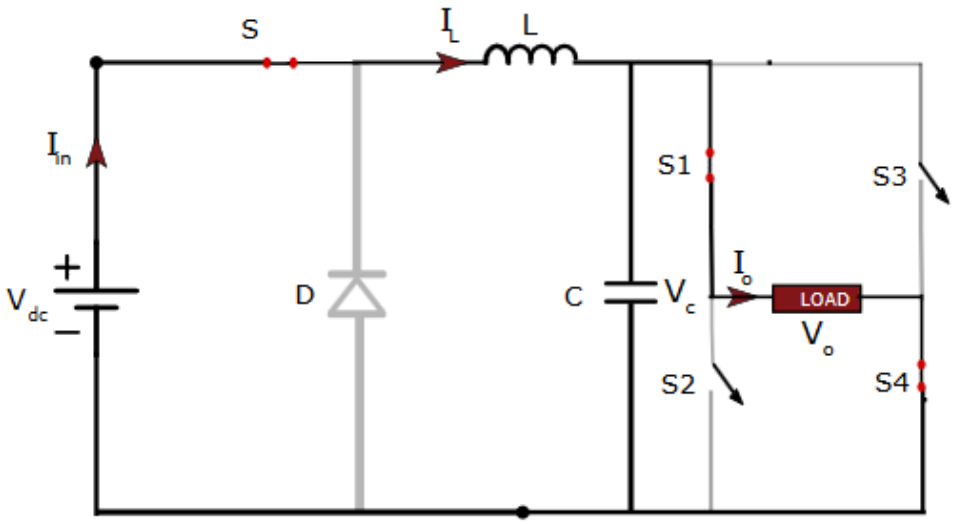

Figure 3.2 Mode I operation of ILI

Mode II

In this mode, the switch S will be in OFF state and the diode D gets forward biased. The inductor gets discharged in this mode and the load voltage will be positive. The current path will be through the switches $S_1$and S_4.Figure 3.3 shows the circuit operation in mode II

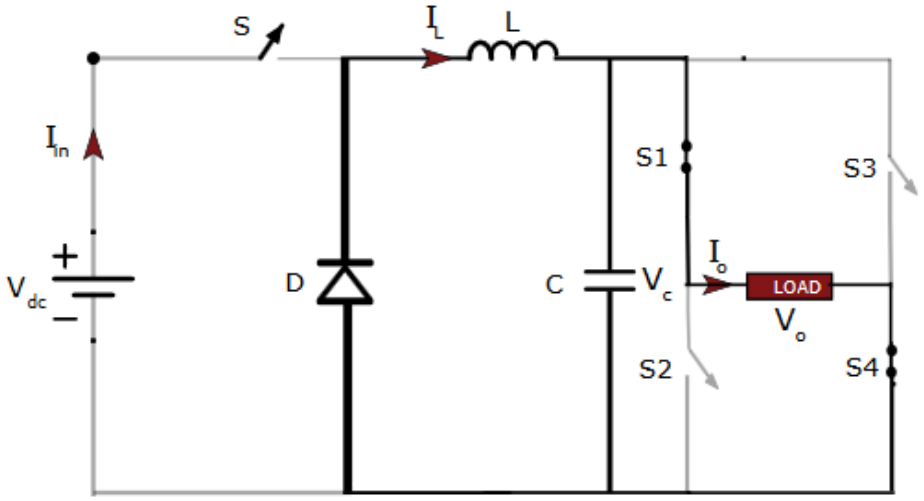

Figure 3.3 Mode II operation of ILI

Mode III

Mode III and IV are defined for negative half cycle**.** In mode III, the inductor L gets charged. Since the switches S_2 and S_3 of the H-bridge inverter are ON, the current and voltage polarity will be negative. Figure 3.4 represents the operation of the circuit in mode III.

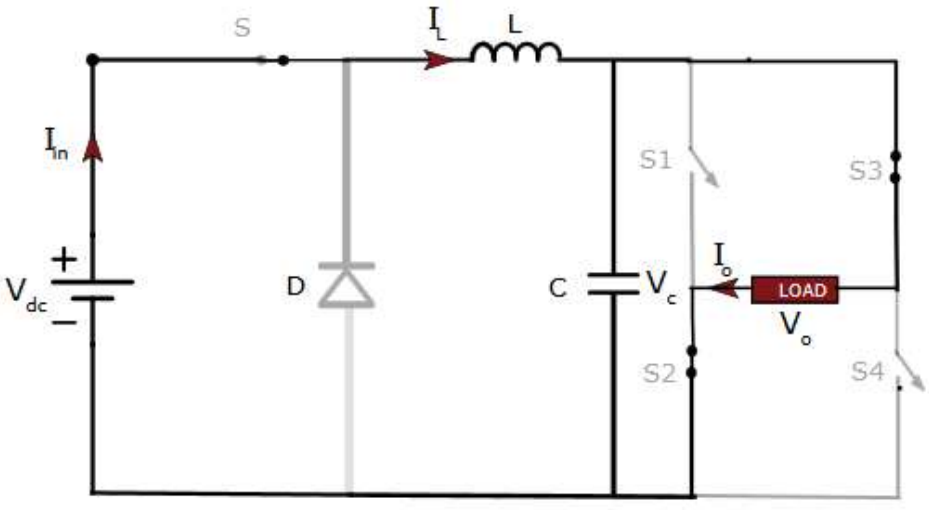

Figure 3.4 Mode III operation of ILI

Mode IV

The high frequency switch S is OFF condition. The stored energy in the inductor will be discharged through switches S_2 and S_3 in the negative direction. The diode D will be forward biased in this mode.

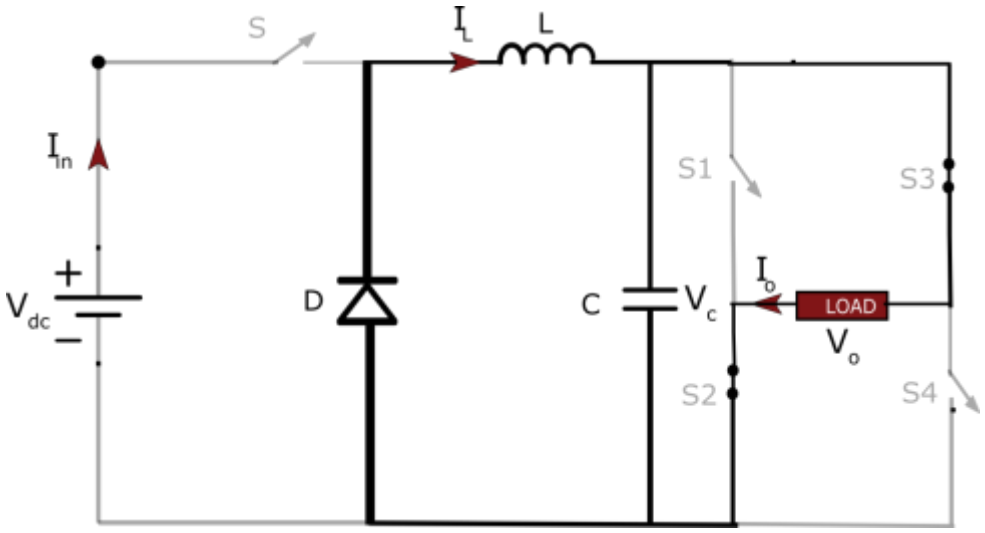

Figure 3.5 Mode IV operation of ILI

3.3. Three Phase Infinite Level Inverter

Three phase infinite level Inverters are derived from the single phase switched mode inverter and poses various advantages over multilevel inverters. The high DC bus utilization along with low harmonic output voltage is the most commendable feature of the three phase ILI (TILI).The TILI can be used as the driving inverter for a motor, can be employed in reactive power compensation circuits and can be utilized for the grid integration of renewable power sources. It can operate the motor drives in the medium voltage and power levels. Figure 3.6 below shows the circuit diagram of the three phase Infinite Level Inverter. Three separate single phase ILI modules are used to obtain the three phase ILI. The load employed is star connected resistive load. The operating mode of TILI is similar to single phase ILI extended to three phases with proper phase shifting of switching pulses.

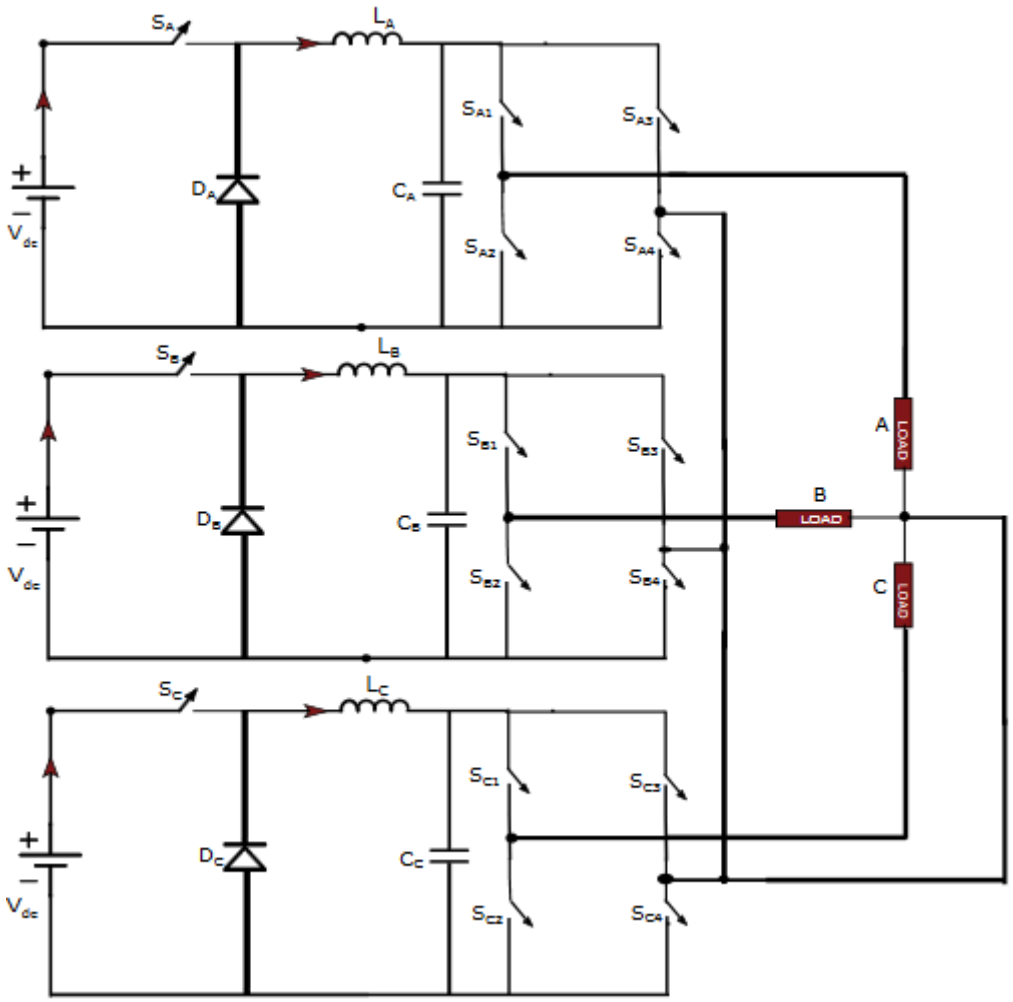

Figure.3.6.Three phase Infinite Level Inverter

From equation (3.2); it is can be seen that duty ratio d is varied by comparing a rectified sine wave with a high frequency carrier wave. This gives a sine PWM signal. Output voltage equation across the buck converter for three phases can be written as follows,

Let d_a, d_b & d_c be the duty ratios of PWM pulses for A phase, B phase &C phase respectively.

Since rectified sine PWM is applied we can write for the three phase system,

$$d_a = D_a|sin\omega t| \tag{3.4}$$

$$d_b = D_b \left|\sin(\omega t - \frac{2\pi}{3})\right| \tag{3.5}$$

$$d_c = D_c \left|\sin(\omega t + \tfrac{2\pi}{3})\right| \quad (3.6)$$

By applying the above duty ratio command to the three buck switches of the three phases we can obtain the capacitor voltage as,

$$V_{ca} = d_a V_{dc} \quad (3.7)$$

Since DC input will be equal to the maximum value of output, we can write, $V_{dc} = V_m$ and substituting for d_a from (3.4), (3.7) becomes,

$$V_{ca} = D_a V_m |Sin\omega t| \quad (3.8)$$

$$V_{cb} = D_b V_m \left|Sin(\omega t - \tfrac{2\pi}{3})\right| \quad (3.9)$$

$$V_{cc} = D_c V_m \left|Sin(\omega t + \tfrac{2\pi}{3})\right| \quad (3.10)$$

For a balanced three phase system, the duty ratios D_a, D_b & D_c should be equal which is given by D.

From the equations(3.8) to (3.10) the output voltages across the three phases of buck converters; are a rectified sine wave with peak amplitude as the DC input and phase angle displaced by $\frac{2\pi}{3}$ radians with respect to each other. The corresponding H-bridges following the buck converters are synchronized with reference signals and operate at fundamental frequency to unfold the capacitor voltages into a pure sinusoidal wave. If the phase A is considered for the analysis, pair of switches (S_{Al}, S_{A4}) and (S_{A2}, S_{A3}) are switched on and off with respect to their fundamental reference waveform. For positive half cycle of the fundamental reference wave form, switches (S_{Al}, S_{A4}) are switched ON and it will operate for half time period. In the negative half cycle, Switches (S_{A2}, S_{A3}) are turned on and the output voltage will be sinusoid with negative values. The obtained phase voltages are given as,

$$V_a = DV_m Sin\omega t \quad (3.11)$$

$$V_b = DV_m Sin(\omega t - \tfrac{2\pi}{3}) \quad (3.12)$$

$$V_c = DV_m Sin(\omega t + \tfrac{2\pi}{3}) \quad (3.13)$$

For maximum output voltage, D is selected as 1. The switches in H-bridge are switched at a very low frequency compared to the switch in buck converter. Thus the switching loss in the H-bridge switches is negligible compared to the high frequency switching device in buck converter. Equations (3.11-3.13) are the equation of phase voltages. These three sinusoidal voltages are $\frac{2\pi}{3}$ radians phase shifted with respect to each other and peak amplitude as that of input DC voltage. The output voltage level depends upon the switching frequency and since the switching frequency very high compared to the fundamental frequency, the voltage level approaches infinity. Since the output voltage level is varying in sinusoidal manner, the obtained voltages across the load have less distortion. When operated with balanced three phase resistive load; operation is same as a three phase voltage source inverter with pure sinusoidal output supplying balanced loads. It can operate with or without neutral thus facilitating three phase three wire system.

The line voltages can be represented as,

$$V_{ab} = \sqrt{3}DV_m Sin(\omega t + \frac{\pi}{6}) \quad (3.14)$$

$$V_{bc} = \sqrt{3}DV_m Sin(\omega t - \frac{\pi}{2}) \quad (3.15)$$

$$V_{ca} = \sqrt{3}DV_m Sin(\omega t + \frac{5\pi}{6}) \quad (3.16)$$

So the peak value of output voltage is given by

$$V_{peak} = \sqrt{3}DV_m$$

Taking $D = 1$,

$$V_{peakl} = \sqrt{3}V_m$$

$$V_{rmsl} = 1.23V_{dc} \quad (3.17)$$

So the DC bus utilization is high compared with Sine PWM VSI and SVPWM VSI. For obtaining a line –line RMS voltage of 400V only 325V DC is to be applied.

To obtain a fundamental line voltage RMS voltage of 400V, The DC input voltage required for a three phase VSI operating under 180 degree conduction mode is given by the equation,

$$V_{l(rms)} = \frac{4V_s}{\sqrt{2}\pi} sin\,{}^{\pi}/_{3}$$

$$V_s = \frac{\sqrt{2}\pi \times 400}{4 \times sin\,{}^{\pi}/_{3}}$$

$$V_s = 512V(dc)$$

For Sine PWM inverter; the DC input voltage required can be obtained from the relation,

$$V_{l(rms)} = \frac{\sqrt{3}V_s}{2\sqrt{2}}$$

$$V_s = \frac{400 \times 2\sqrt{2}}{\sqrt{3}} = 654V(dc)$$

For 3rd harmonic injection or space vector pulse width modulated inverter (SVPWM) to obtain 400V RMS line to line voltage; the DC voltage required can be obtained from the relationship,

$$V_{l(rms)} = \frac{\sqrt{3}V_s \times 1.154}{2\sqrt{2}}$$

$$V_s = \frac{400 \times 2\sqrt{2}}{\sqrt{3} \times 1.154} = 564V(dc)$$

Compared to the sine PWM inverter; 3rd harmonic injection or SVPWM inverter increases the amplitude by 15.4% and thus the DC voltage is reduced by 15.4%. From the inverters listed above; it is found that the ILl has the least DC bus voltage (half of sine PWM & 0.576 times of SVPWM) and highest DC link-utilization.

3.4. Simulation of Conventional ILI

To investigate the theoretical performance, the conventional infinite level inverter is simulated using Matlab/Simulink. Both singe phase ILI and three phase ILI is simulated. The simulation parameters are given in the Table 3.1.

Table 3.1.Simulation Parameters of Conventional ILI

Parameters	***Values***
Input Voltage, Vs	325V
Inductor, L	20mH
Capacitor, C	.6 μF
Switching Frequency, fs	10kHz
Load Resistance, R	100Ω

3.4.1. Simulation of Single phase ILI

The single phase ILI is simulated with above parameters. The simulated waveforms of output voltage, output current, inductor current input and input current are given in Figure 3.7.

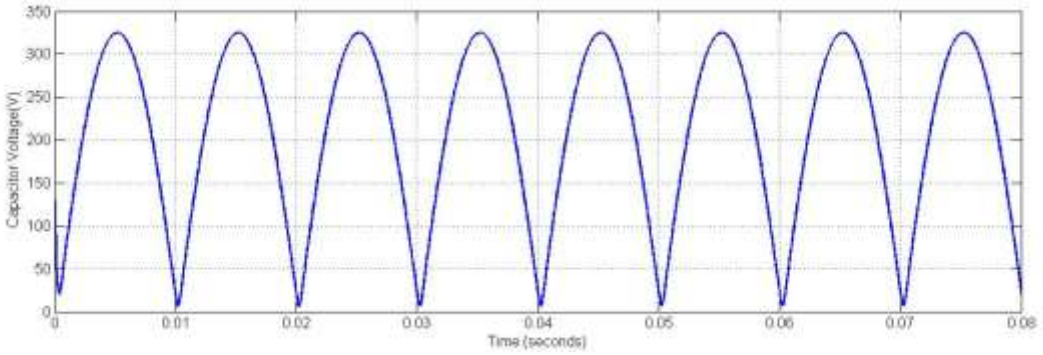

Figure 3.7 (a).Voltage across the capacitor of conventional ILI

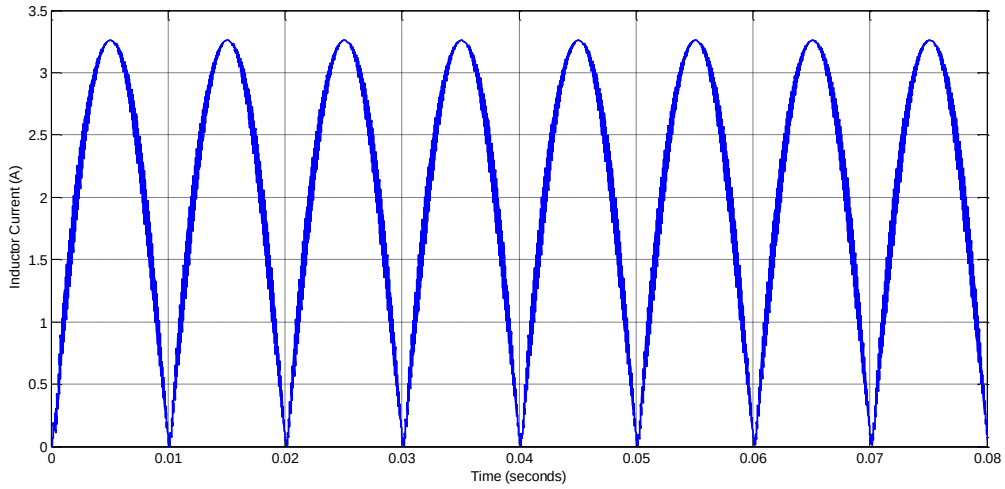

Figure 3.7(b). Inductor current waveform of conventional ILI

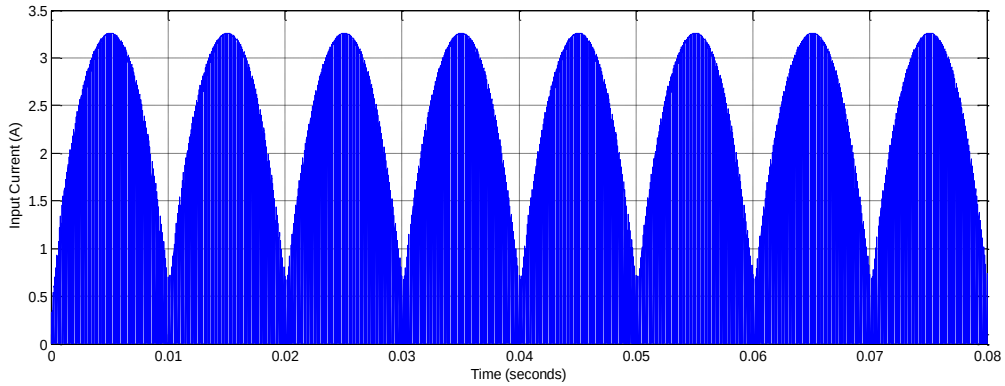

Figure.3.7(c) Input current waveform of conventional ILI

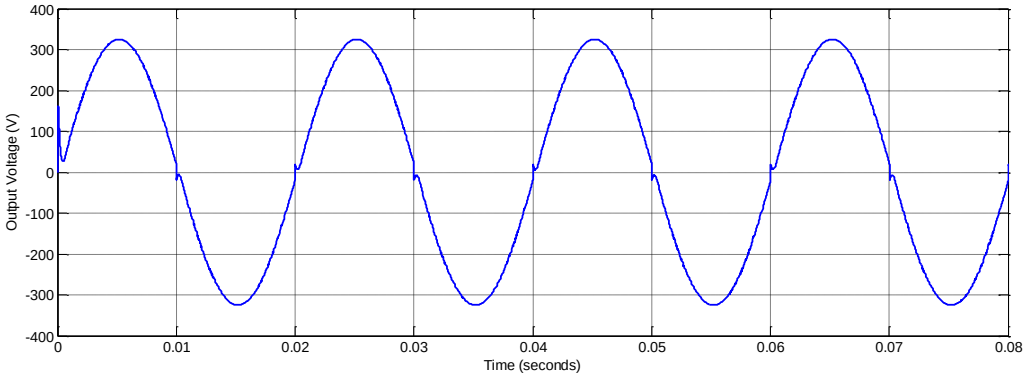

Figure 3.7 (d) Output voltage of single phase ILI

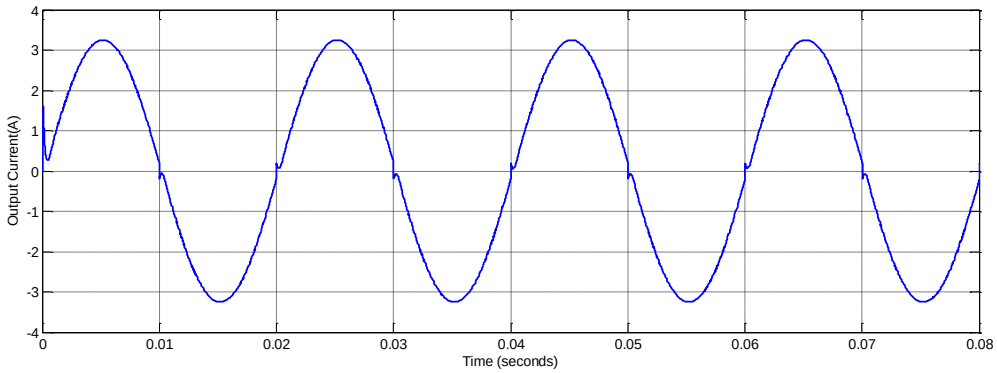

Figure.3.7(e) Output current waveform of conventional ILI

The obtained voltage output is sinusoidal in nature and the inductor current and input current are fully rectified sine waves. At the zero crossing instances, there are ripples due to the unfolding operation done by H-bridge section.

Figure .3.8 shows the FFT window of the output voltage. From the s, it can be seen that for given parameters, output voltage THD of ILI is obtained as 1.66%.

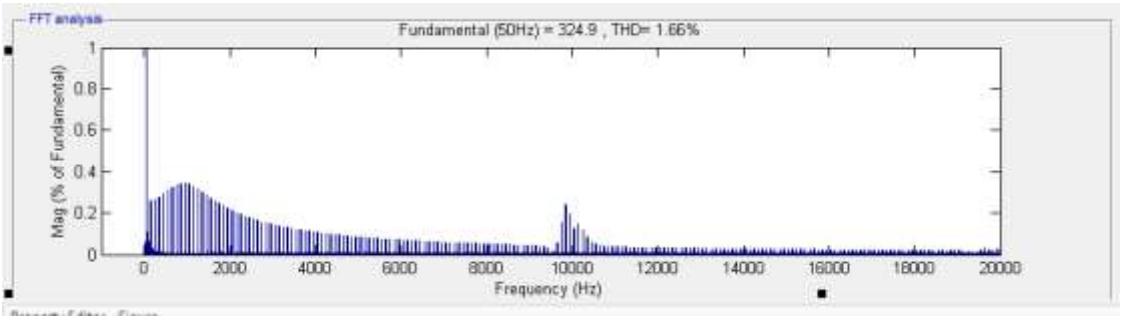

Figure.3.8. Frequency spectrum of output voltage of single phase ILI

3.4.2. Simulation of Three Phase Infinite Level Inverter

Three phase inverter is simulated with star connected balanced load. The simulation parameters are the same as given in Table I. For RL load simulation, inductance of 1mH is chosen. Simulation results showing phase voltage, phase current and line voltage is given in Figure 3.9.

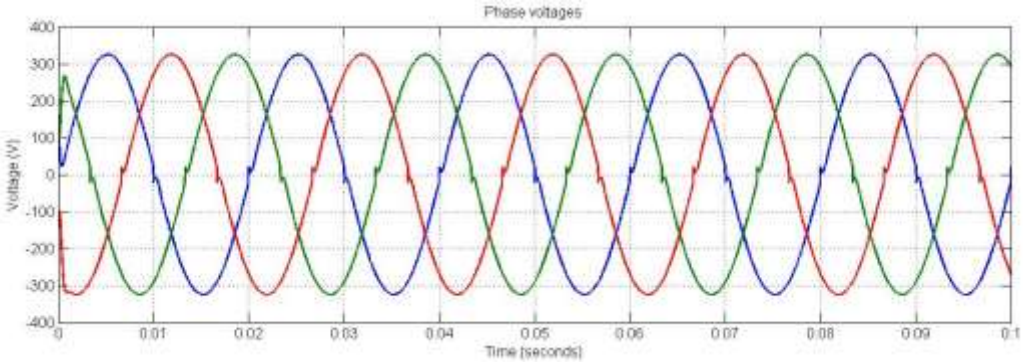

Figure.3.9. (a) Phase Voltage waveform of Conventional ILI

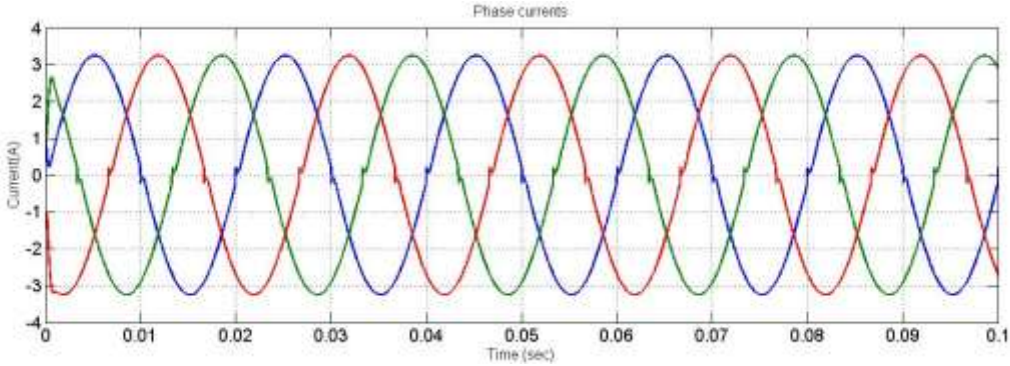

Figure.3.9(b) Phase Current waveform of conventional ILI

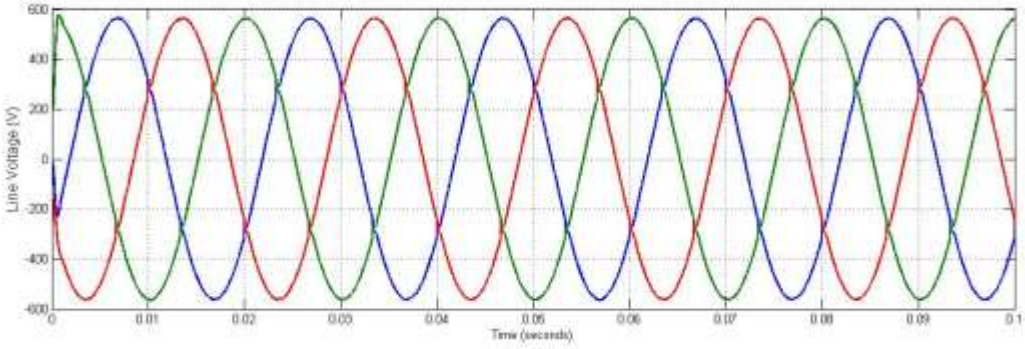

Figure.3.9(c) Line Voltage waveform of conventional ILI

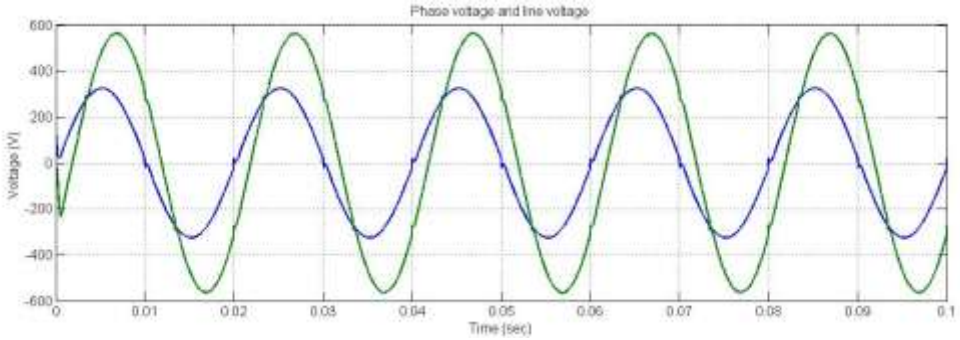

Figure.3.9. (d) Line voltage and phase voltage waveform of conventional ILI

Figure.3.9. (a) shows the phase voltage waveform of conventional ILI. The peak value is the DC link voltage itself given as 325V. The RMS value obtained is 230V. Figure.3.9. (b) shows the phase current waveform of conventional ILI. Figure 3.9(c) represents the line voltage waveform. The line voltage wave form clearly indicates that with given input DC voltage of 325V, the peak value of output line voltage is 565V which is high in comparison with the VSI with sine PWM and SVPWM. The RMS value of line voltage is obtained to be near to 400V. Figure.3.9. (d) shows the phase voltage and line voltage waveforms indicting the phase difference of 30^0 between both. The obtained voltages are balanced and giving high DC bus utilization in comparison to the existing topologies. For a balanced resistive load, the output obtained is of high quality sinusoidal nature with phase voltage THD of 1.59% (Figure3.10.(a)). The line voltage THD is obtained to be 1.28% (Figure 3.10.(b)) and the phase current THD is 1.59%. (Figure 3.10(c)).

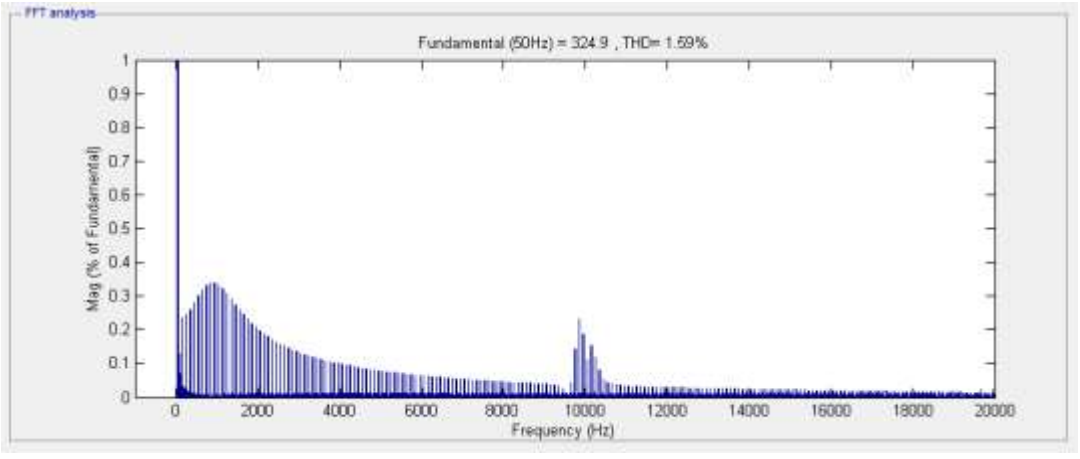

Figure 3.10(a). Frequency spectrum of phase voltage using FFT analysis (R load)

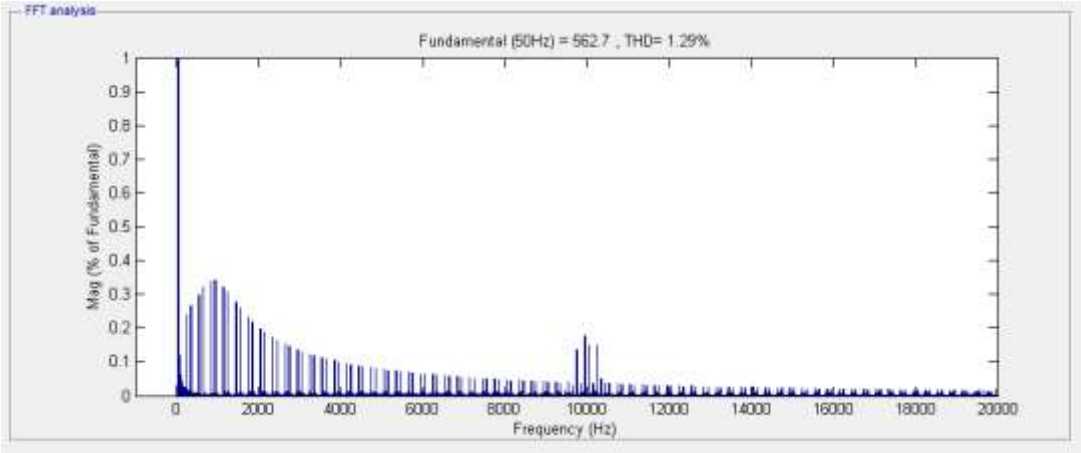

Figure.3.10.(b). Frequency spectrum of line voltage using FFT analysis(R load)

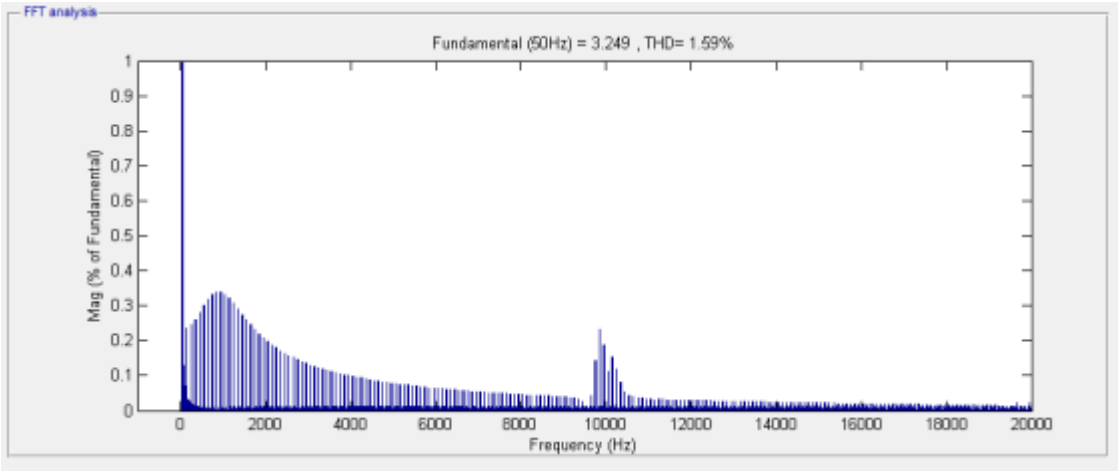

Figure.3.10(c) Frequency spectrum of phase current using FFT analysis.(R load)

The frequency spectrum of phase voltage, phase current and line voltage for RL load is shown in Figure 3.11. It can be seen that the THD of phase voltage under RL load condition is 1.66 % (Figure 3.11(a)). The line voltage has a THD of 1.36% (Figure 3.11(b)) and phase current has THD of 1.59 %(Figure 3.11(c)).

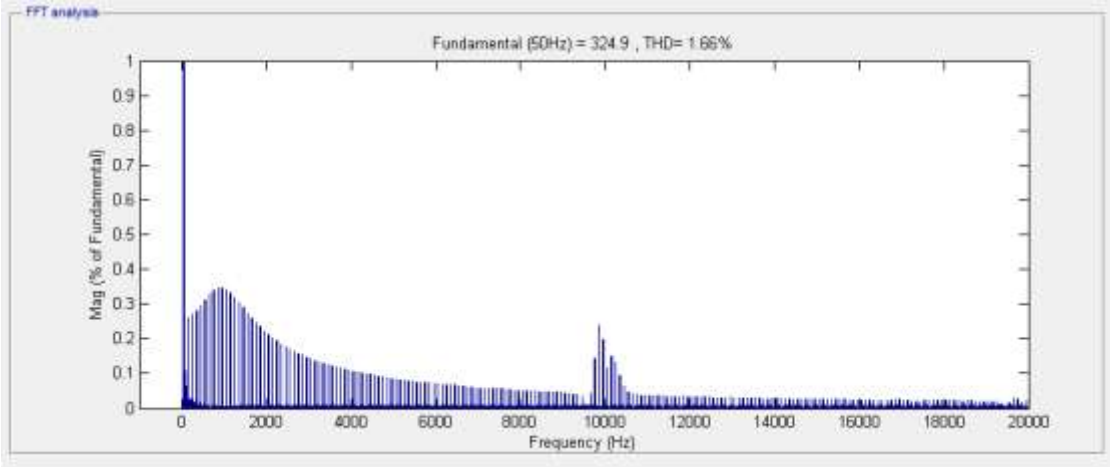

Figure 3.11(a) Frequency spectrum of Phase voltage using FFT analysis (RL load)

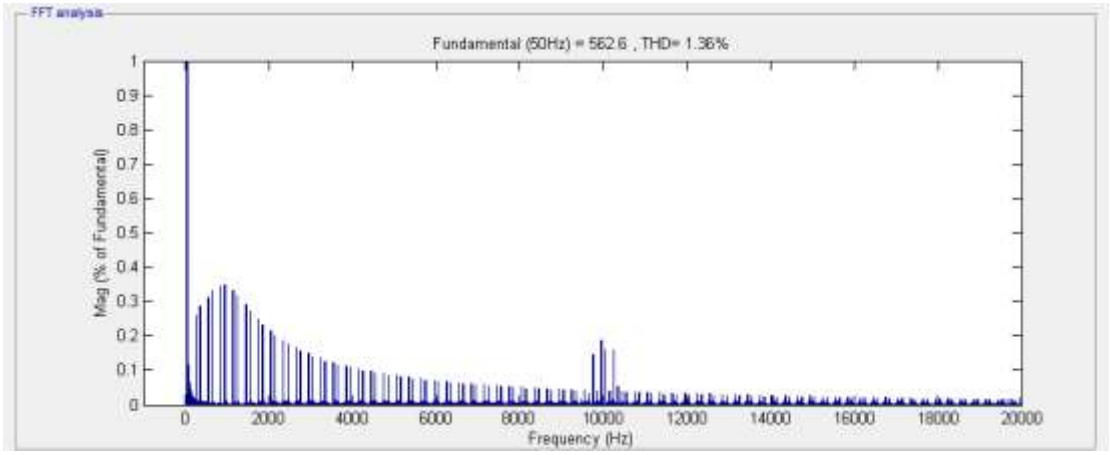

Figure 3.11(b) Frequency spectrum of Line voltage using FFT analysis (RL load)

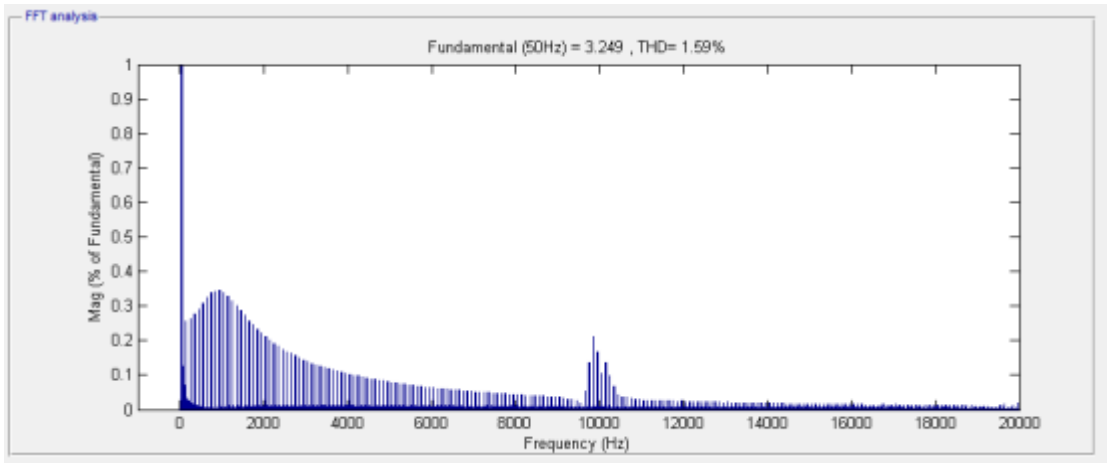

Figure 3.11(c) Frequency spectrum of phase current using FFT analysis (RL load)

It can be concluded that the quality of output obtained from this ILI topology is within the IEEE standards (<5%). Even under various load conditions the THD obtained is less than 2% which indicate that the inverter can be a better candidate for use under critical loads seeking high quality.

Table.3.2. shows the comparison of THD values of phase voltage, line voltage and phase current under resistive load and RL load.

Table.3.2. Comparison of THD with different load conditions

Output Waveform	**R Load**	**RL Load**
Phase Voltage	1.59%	1.66%
Line Voltage	1.29%	1.36%
Phase Current	1.59%	1.59%

3.5. Features of Infinite Level Inverters

- Since the DC bus utilization is more, voltage stress across the devices is less increasing the reliability of the inverter.
- No dead time required in the switching since shoot through problem is eliminated.
- DC capacitor (electrolytic type) is used here which is less bulky than AC capacitors.
- More number of capacitors switches and diodes are a major drawback of multilevel inverter. But device count is the minimum for the infinite level inverters.
- Unlike conventional MLI, the output voltage level depends upon the switching frequency.
- The advanced control techniques which are applicable to normal DC-DC converters can be used to control ILI.
- The harmonics in the output voltage is very less and within permissible limits.
- Since only one switch per phase is operating at high frequency and all the switches of H-bridge is operating at fundamental frequency the switching loss is

considerably less. Also, the H-bridge switches are operating under zero voltage switching (ZVS) which will reduce the power loss further.

3.6. Disadvantages of the Conventional Infinite Level Inverter

- Each phase poses one extra active and passive switch making the circuit more complex.
- The conduction loss is more due to the presence of the extra switches.
- The unfolding of the fully rectified sine wave voltage at the output of the buck converter will create notches at the zero crossing point. This will affect the quality of the output voltage.
- The circuit lack bidirectional power flow capability making it not suitable for battery charging and grid tied operations.

3.7. Summary

In this chapter, conventional infinite level inverter is described in detail. ILI gives a near sinusoidal output making the term infinite level meaningful. Three phase infinite level inverter is derived from the single phase infinite level inverter and is having better DC bus utilization compared with the conventional VSI with sine PWM and SVPWM. Compared to multilevel inverter topologies, ILI has the minimum number of switches and passive elements. Also, no additional filtering circuit is required. FFT analysis of voltage and current under different load natures is also analyzed. THD is well within the IEEE standards and the ILI is a better candidate for critical application. Conventional ILI has redundancy in terms of number of switches and the output voltage contains ripples at the zero crossing instances due to the unfolding of rectified sine wave. Reduction in switch count will reduce the switching loss and also the cost of the inverter can be considerably reduced. In the next chapter a novel Infinite level inverter is discussed which is having reduced number of switches and poses better output quality as compared to conventional ILI.

Chapter 4

Novel Four Switch Infinite Level Inverter Topology

4.1. Introduction

Conventional infinite level inverters have low harmonics in the output and high DC bus utilization. Most of the problems associated with multilevel inverters are eliminated by ILI topologies. Conventional ILI requires front end circuit with one high frequency switch and diode per phase. Overall 15 switches are needed in Three phase infinite level inverter thus losses and size of the inverter will be more. In this chapter a novel four switch infinite level inverter is proposed. The proposed topology has only one inductor and capacitor per phase thus reducing the size, weight and cost of the system. A sinusoidal varying duty ratio PWM control is implemented here which provides inherent buck operation. Only one switch is operating at high frequency ensuring that switching loss is same as in conventional ILI. No additional diode and high frequency switch is required in proposed topology. Distortion at the zero crossing instances present in the conventional ILI is eliminated here since for each half cycle, separate circuits are in operation.

Outline of the chapter is as follows. In section 4.2., concept of proposed novel four switch infinite level inverter (FSILI) and its various features are explained. In section 4.3, steady state analysis of the FSILI is done. Control implementation of proposed FSILI both under open loop and closed loop is explained in section 4.4. Section 4.5 gave the simulation study and analysis of results. Chapter is concluded in Section 4.6.

4.2. Proposed Novel Four Switch Infinite level inverter (FSILI)

Proposed topology is a modification to the existing infinite level inverter topology explained in the last chapter. The conventional single phase ILI has 5 switches where as in the proposed topology, only four switches are employed. Here, the duty ratio is a time

varying function and it changes in each switching cycle, which is equivalent to change in the output voltage level with switching duty. If f_o is the fundamental frequency of output voltage and f_s is the switching frequency, then f_s/f_o will give the number of possible levels in the output voltage. Since duty ratio is a sine function, which is varied in every switching cycle, output voltage levels will also vary accordingly. As the switching frequency is very high, the output voltage will be considered to have infinite levels and the inverter can be termed as an infinite level inverter.

The circuit diagram of proposed FSILI is shown in Figure. 4.1. Circuit with only four switches, one inductor, one capacitor and a single DC source comes to be simple, less bulky and cheaper. Switches S1 and S3 operates at high frequency for positive and negative half cycle respectively. Switches S2 and S4 operates at fundamental frequency along with S1 and S3 in positive and negative half cycles each. The shoot through problem present in conventional VSI is eliminated here since the inductor is present in the circuit operation which will limit the sudden rise in current. Effectively only one switch operates at high frequency ensuring the switching loss to be same as the conventional ILI. Additionally, since each switch is operated for half of the fundamental period, the effective switching duty is less, increasing the life of the switch used. The antiparallel diodes of low frequency switches will take part in the circuit operation. Since the antiparallel diodes of low frequency switches are in operation, there will not be any issue of reverse recovery time and thus the circuit can be operated at higher frequencies. Two separate buck circuits are operational in each half cycle.

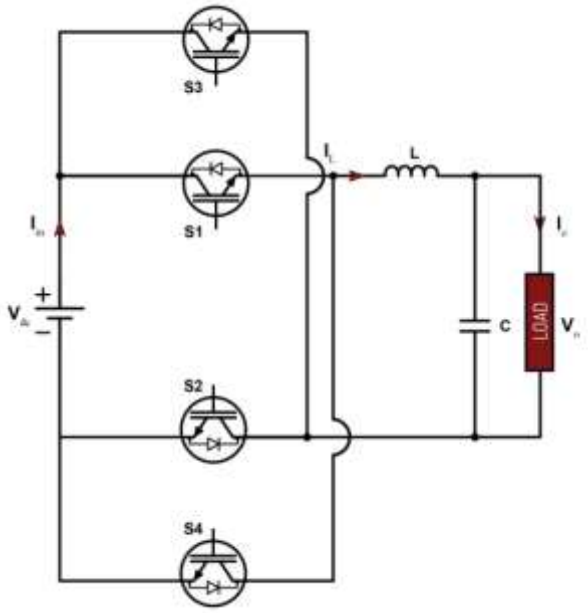

Figure.4.1. Circuit Diagram of Novel Four Switch Infinite Level Inverter

4.2.1. Features of Novel Four Switch Infinite Level Inverter

Main features of the proposed topology

1. The inverter requires only four switches thus size, circuit and control complexity is reduced.
2. Only single capacitor and inductor is required unlike multilevel inverters. The overall size and thus weight and cost are less in comparison with multilevel inverter topologies and conventional ILI.
3. Only one switch operates at high frequency at a particular instant. In the four switches available two are high frequency switches but each operates in half of the fundamental time period only. This is equivalent in terms of switching loss to one high frequency switch operation. But the switching duties on the switches are half only. Thus, the proposed Four Switch ILI has minimum switching loss and switching stress compared to conventional ILI.
4. Since the output voltage level depends upon the switching frequency and is following the sinusoidal modulated signal, it can be seen that the obtained output voltage has least harmonics without any additional filtering requirements.

5. Unlike conventional ILI, a complete sinusoid is taken as modulating reference and separate switching circuits comes into operation for positive and negative half cycles. Thus the unfolding issue using H-bridge inverter is not present here making the output further distortion free.

4.2.2. Operation of Novel Four Switch Infinite Level Inverter

There are four distinct modes in the operation of Novel Four Switch Infinite Level Inverter (FSILI) - Mode I & Mode II for positive half cycle of output voltage, Mode III & Mode IV for negative half cycle. For, $V_o > 0$ and $V_o < 0$ two separate buck circuits are in operation. Figure 4.2 shows the equivalent circuits corresponding to the four modes of operation.S_1 and S_3 are the high frequency switches for positive and negative half cycles respectively whereas S_2 & S_4 are the fundamental frequency switches.

For $V_o > 0$(Figure 4.2.(a) and Figure 4.2.(b)), S_2 is remains turned on and S_1 operates with modified Sine PWM where the duty cycle varies as a sine function while S_3 & S_4 are in off condition. Similarly, for $V_0 < 0$ (Figure 4.2(c) and Figure 4.2(d)), S_4 remains on and S_3 operates with Sine PWM. In this interval, S_1 and S_2 are kept idle.

Mode I*:* In mode I, S_1 & S_2 are in ON condition while S_3 & S_4 are switched OFF. Inductor (L) gets charged through S_1, S_2, and load as shown in Figure 4.2(a). Load voltage will be positive in this mode.

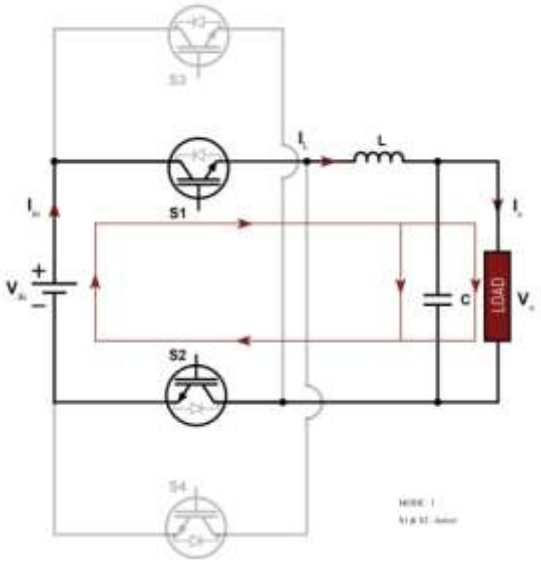

Figure 4.2 (a) Mode I operation of proposed FSILI (Positive half cycle)

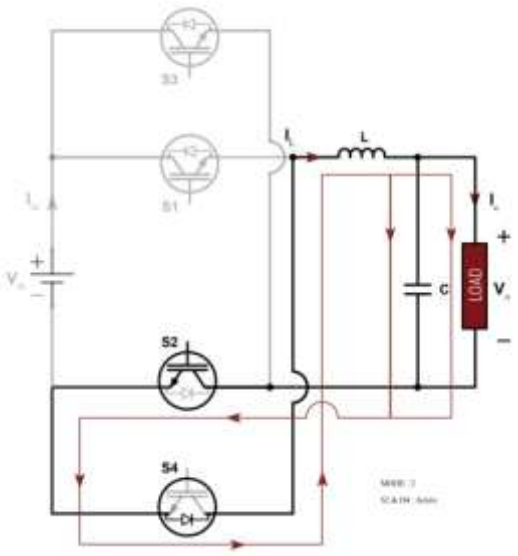

Figure.4.2. (b) Mode II operation of Proposed FSILI (Positive half cycle)

Mode II*:* In mode II, S_2 kept ON while S_1, S_3 & S_4 are in OFF condition. Body diode of Switch S_4 gets forward biased and inductor discharges through body diode of S_4 and switches S_2. Indictor will act as a source and feeds the load and capacitor to give positive voltage. The current path in this mode is shown in Figure 4.2(b).

Mode III*:* In mode III, S_3 & S_4 are in ON condition while S_1 & S_2 are in OFF state. The current path for the inductor to charge is given in Figure.4.2(c). Switch S_3, load inductor L and switch S_4 take part in the operation. A negative load voltage and current is obtained in this mode.

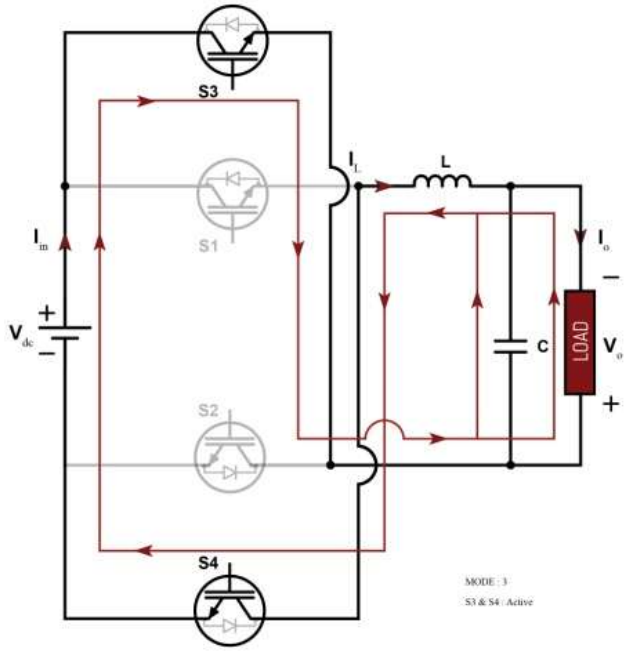

Figure 4.2 (c) Mode III operation of proposed FSILI (Negative half cycle)

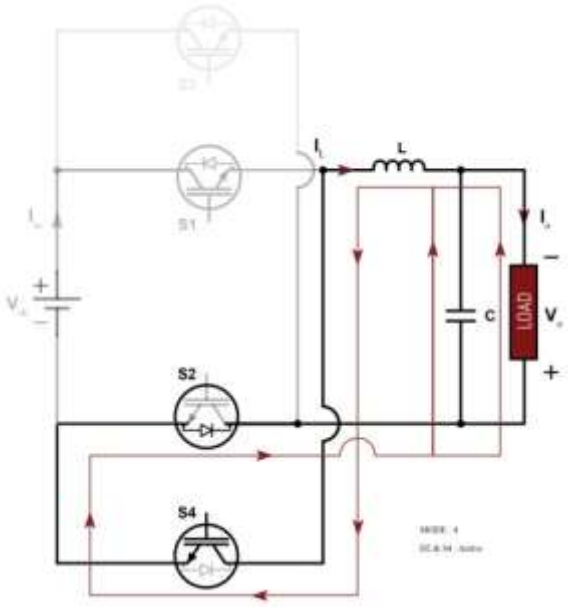

Figure.4.2. (d) Mode III operation of proposed FSILI (Negative half cycle)

***Mode IV*:** In this mode, switch S_4 is ON. S_1, S_2 and S_4 are in OFF condition. Body diode of Switch S_2 gets forward biased and inductor discharges in the negative direction

through S_4, body diode of S_2 and the load. Output voltage will be negative in this mode. The current path in this mode is shown in Figure. 4. 2.(d).

4.3. Steady-State Analysis of Novel Four Switch Infinite Level Inverter

In this section steady state analysis of the proposed inverter is carried out. Input-output relationship is deduced from the analysis. Design equations of inductor and capacitor are also obtained by analyzing waveforms.

4.3.1. Steady-State Voltage Gain

The steady state analysis is carried out with certain assumptions.

1. For a particular switching period, duty ratio and output voltage remains constant.
2. Switching frequency is very much greater than the output ac voltage frequency

From the section 4.2., on analysis of the modes of operation it is clear that the inductor current rises in positive direction during mode I and falls during the mode II. Similar is the case for mode III and mode IV but the difference is that the inductor current variation is in negative half cycle. The analysis and design of the proposed inverter is done for continuous conduction mode (CCM) since the inductor current ripple is the minimum in CCM and also the gain is high in comparison with discontinuous conduction mode (DCM).

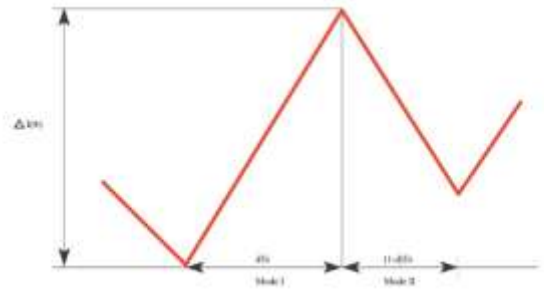

Figure.4.3.Inductor current during a switching cycle

Variation of inductor current during a switching cycle is shown in Figure.4.3. Analysis is done for one switching cycle in the positive half cycle. The same is applicable to negative half cycle also.

The modulation scheme applied here is a modified sine PWM modulation. So it can be written as

For the k^{th} switching cycle, on time,$T_{on} = \mathrm{dT_s}$. where, $d = Dsin\omega t$.

Applying KVL in mode I equivalent circuit, we have,$v_L = V_{dc} - v_o$, where $V_{dc}$is the input DC voltage.

From the above equation, Inductor current ripple at k^{th} switching cycle shown in Figure.4.3 is obtained as

$$\Delta \mathrm{I}(\mathrm{t_k}, \omega t) = \frac{(V_{dc} - v_o)}{L}\, dT_s \tag{4.1}$$

Similarly, during off time (Mode II),$T_{Off} = (1-d)T_s$, of k^{th} switching cycle.

Applying KVL in this mode, $v_L = -v_o$,

So, inductor current ripple at k^{th} switching cycle can also be expressed as

$$\Delta \mathrm{I}(\mathrm{t_k}, \omega t) = \frac{v_o(1 - dT_s)}{L} \tag{4.2}$$

From Eq. (4.1) & Eq. (4. 2), it can be written as

$$\frac{(V_{dc} - v_o)}{L}\, dT_s = \frac{v_o(1 - dT_s)}{L} \tag{4.3}$$

Solving the above equation we get,

$$V_{dc}\, dT_s = v_o \tag{4.4}$$

$$v_o = V_{dc} D sin\omega t \tag{4.5}$$

$$Dsin\omega t = \mathrm{d} = \frac{v_o}{V_{dc}} \tag{4.6}$$

Analysis clearly indicates that the inverter is buck derived topology with a sine modulated output. Buck nature ensures linear relationship between input and output voltages and pure sinusoidal output can be obtained in the output. In case of boost and buck boost inverter topologies, linearization techniques need to be incorporated to get sinusoidal output.

4.3.2. Inductor Design

We have peak to peak ripple voltage given by equation 4.1 as

$$\Delta I(t_k) = \frac{(V_{dc}-v_o)d}{L*f_s}$$

$$\Delta I(t_k) = \frac{(V_{dc}-v_o)v_o}{L*f_s*V_{dc}}$$

$$\Delta I(t_k) = ((V_{dc} * v_o - {v_o}^2))/(L * f_s * V_{dc}) \quad (4.7)$$

If RMS output voltage is represented as V_o , output voltage can be expressed as $v_o = \sqrt{2}V_o\, Sin\omega t$

Thus peak to peak ripple inductor current of k^{th} switching cycle of the high frequency switch can be expressed as

$$\Delta I(t_k, \omega t) = (V_{dc} * \sqrt{2}V_o\, sin\omega t - (\sqrt{2}V_o)^2 sin^2\omega t)/(L * f_s * V_{dc}) \quad (4.8)$$

By conducting second derivative test on the inductor current ripple equation, we can obtain the condition for maximum inductor current ripple.

$$\frac{d}{d\omega t}(\Delta I(t_k)) = 0 \quad (4.9)$$

$$\frac{\sqrt{2}V_o}{L*f_s*Vi}\left[\frac{d}{d\omega t}(V_{dc} * Sin\omega t - \left(\sqrt{2}V_o\, sin^2\omega t\right)\right] = 0 \quad (4.10)$$

$$\frac{\sqrt{2}V_o}{L*f_s*Vi}\left[V_{dc} * cos\omega t - \left(\sqrt{2}V_o\ * 2 * Sin\omega t * cos\omega t\right)\right] = 0 \quad (4.11)$$

Therefore,

$$V_{dc} * cos\omega t = \left(2\sqrt{2}V_o\, Sin\omega t * cos\omega t\right) \quad (4.12)$$

$$V_{dc} = \left(2\sqrt{2}V_o\, Sin\omega t\right)$$

$$Sin\omega t = V_{dc}/\left(2\sqrt{2}V_o\right) \quad (4.13)$$

$\sqrt{2}V_o = V_{dc}$ is the peak value of output voltage which will be equal to the input DC voltage, so they will cancel out.

Therefore, $Sin\omega t = \frac{1}{2}$ and $\omega t = \pi/6$ radians

So, the maximum ripple occurs at π/6 radians. Minimum value of inductance can be selected at this instance.

$$\Delta \mathrm{I}_{\max} = [\left(V_{dc} * \sqrt{2}V_o \ * \frac{1}{2}\right) - \left(\left(\sqrt{2}V_o\right)^2 1/4\right)]/(L_{min} * f_s * V_{dc}) \quad (4.14)$$

$$L_{min} = [(V_{dc} * V_o) - \left(\sqrt{2}(V_o)^2\right)]/(\Delta \mathrm{I}_{\max} * f_s * V_{dc} \quad (4.15)$$

$$L_{min} = V_o\,(\sqrt{2}(V_{dc}) - V_o)/(2 * \Delta \mathrm{I}_{\max} * f_s * V_{dc}) \quad (4.16)$$

By substituting the values of various parameters inductance value can be obtained for the proposed inverter.Equation (4.16) is used for the design of inductance in table 4.1.

4.3.3. Capacitor Design

The capacitor at the output side of the inverter can be designed using the relationship between voltage ripple in the output and charge stored in the capacitor.

Using the equation, $\Delta V_o = \Delta \mathrm{Q}/\mathrm{C}$ the minimum capacitance value required for the circuit operation can be found out.

We have for a buck converter,

$$\Delta Q = \frac{\Delta I(t_k, \mathrm{wt}) T_s}{8}$$

Hence $\Delta V_{o\,\max} = \Delta I_{max}\,/8 f_s\, C_{min}$

Therefore,

$$C_{min} = \Delta I_{max}\,/(8 f_s\ \Delta V_{o\,\max}) \quad (4.17)$$

Using this equation the capacitor is designed, which is listed in Table.4.1.

4.4. Control Implementation of Proposed Infinite Level Inverter

From the analysis it is understood that by properly applying switching pulses, the proposed inverter can be operated to obtain good quality AC output. For this a good control implementation is necessary. The inverter can be operated either in open loop manner or in closed loop manner. Pulses for high frequency operated switches and fundamental frequency switches should be generated with the control implementation. The closed loop control will indicate the transient and steady state behavior of the proposed inverter.

4.4.1. Open loop Control of Proposed Infinite Level Inverter

Open loop control block diagram of proposed FSILI is given in Figure. 4.4. From Equation (4.3), it is clear that as maximum value and thus RMS value of the output voltage is depending on D, output voltage can be controlled by controlling D. Hence modulating signal $d = Dsin\omega t$ is generated using a reference sine wave and is fed to a PWM generator after rectification. The high frequency carrier is compared with the rectified sine modulating signal. A zero crossing detector will generate pulses for S_2 and S_4. The PWM pulse generated by comparison of fully rectified sine wave and triangular carrier wave will be logically ANDed with switching pulse of S_2 to obtain pulse for switch S_1. Similarly switching pulse for S_3 is obtained. The switching pulses obtained are shown in Figure.4.5.

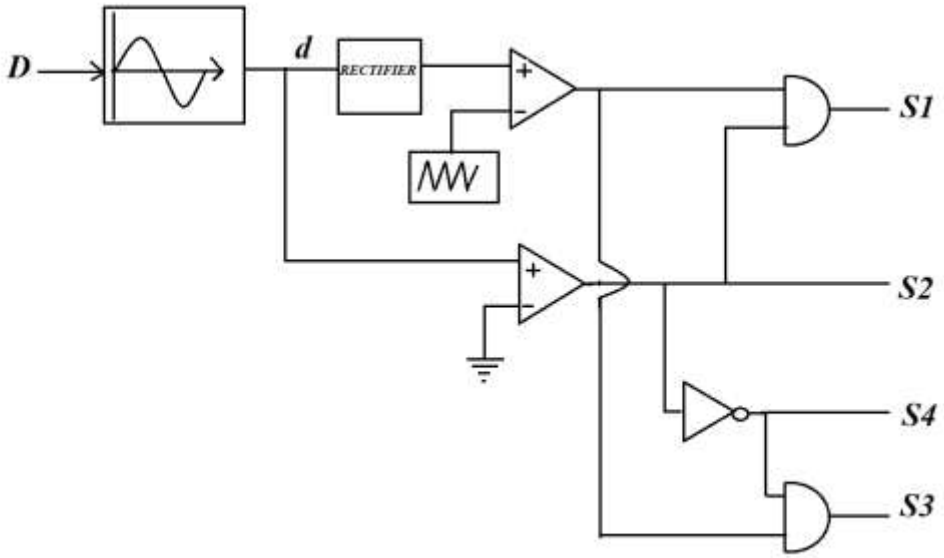

Figure.4.4.Open loop control block diagram of Proposed FSILI

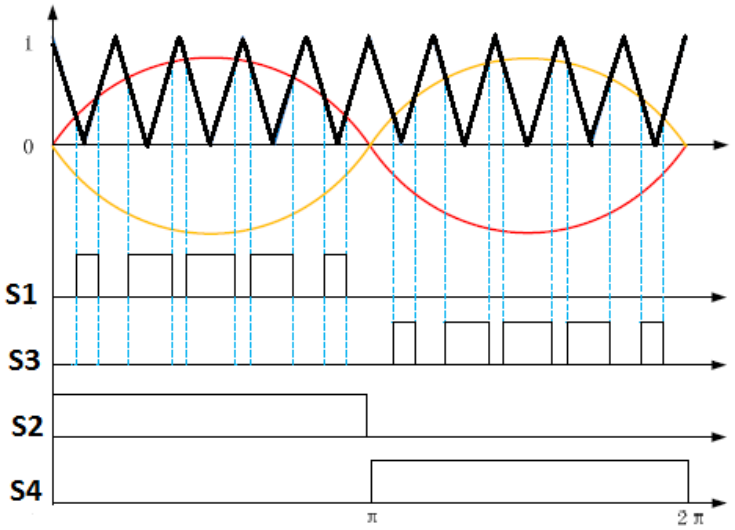

Figure.4.5. Switching pulses for proposed Infinite Level Inverter

4.4.2. Closed Loop Control of Proposed Infinite Level Inverter

In order to eliminate effect of disturbances and to understand the robustness of the system closed loop control of power electronic systems are done. Here, for the proposed FSILI, the closed loop control is done with a PI controller. Since the output voltage is sinusoidal in nature, instantaneous values of output and reference cannot be compared to minimize the error using PI controller. Instead, the actual RMS value of output voltage, $V_{orms}$and RMS value of required output $V_{orms\,ref}$ is compared and the error is fed to the PI controller so that amplitude of sine wave, D is adjusted to obtain the required output voltage. Trial and error method is adopted for tuning the PI controller.

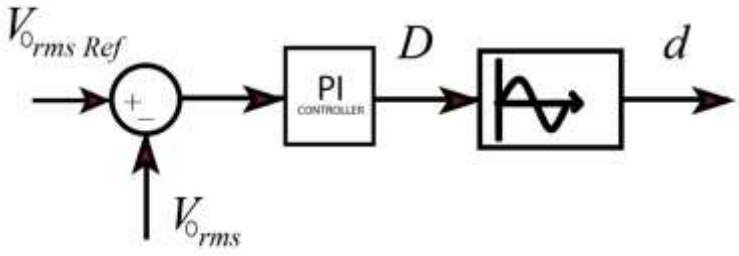

Figure.4.6. Closed loop control of proposed Infinite Level Inverter

4.5. Simulation Results and Analysis

With the parameters given in Table 4.1 simulation of Novel Four Switch Infinite Level Inverter is carried out in Matlab/Simulink. Output voltage, load current, inductor current and input current waveforms are analyzed and THD of output voltage is also investigated.

Table4.1. Simulation Parameters of Novel FSILI

Parameters	***Values***
Input Voltage V_{dc}	325 V
Inductor, L	20mH
Capacitor, C	0.6 μF
Switching Frequency, f_s	10 kHz
Load Resistance, R	100

4.5.1. Open loop Simulation of FSILI

In order to validate the theoretical concept, simulation of FSILI is carried out in open loop. Control pulses applied to the switches of proposed inverter is given in Figure. 4.7. It can be seen that the pulses for S_1 and S_3 are high frequency PWM pulses whereas the pulses S_2 and S_4 are with 20ms time period.

Figure.4.8(a), 4.8(b), 4.8.(c) & 4.8(d) shows the output voltage, load current, inductor current and input current waveforms respectively of the proposed FSILI.

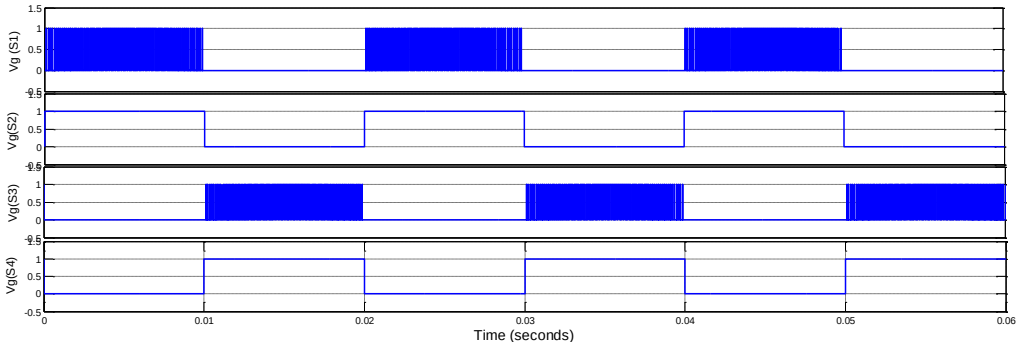

Figure.4.7. Switching pulses applied to Proposed Novel Four Switch Infinite Level Inverter

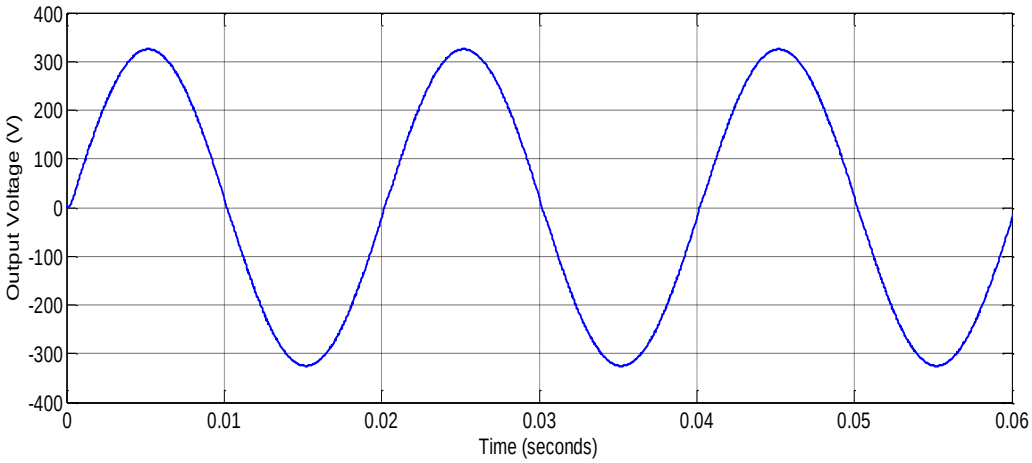

Figure.4.8(a) Output voltage of Novel FSILI.

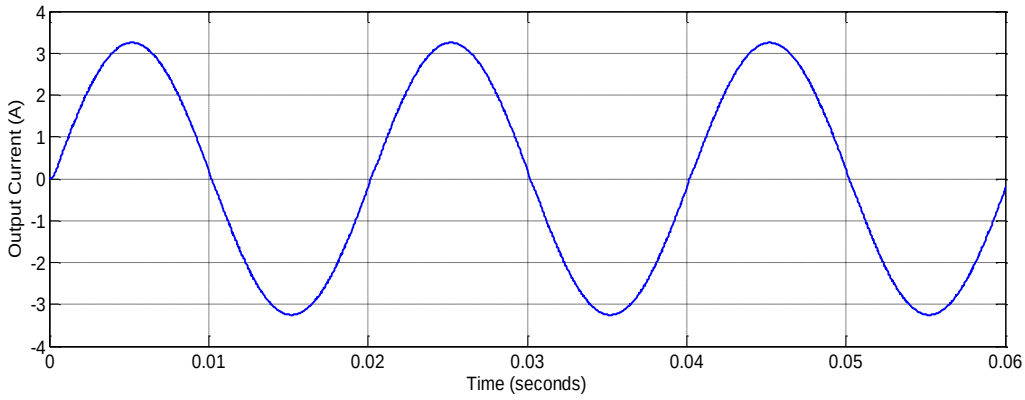

Figure.4.8. (b) Output current of Novel FSILI

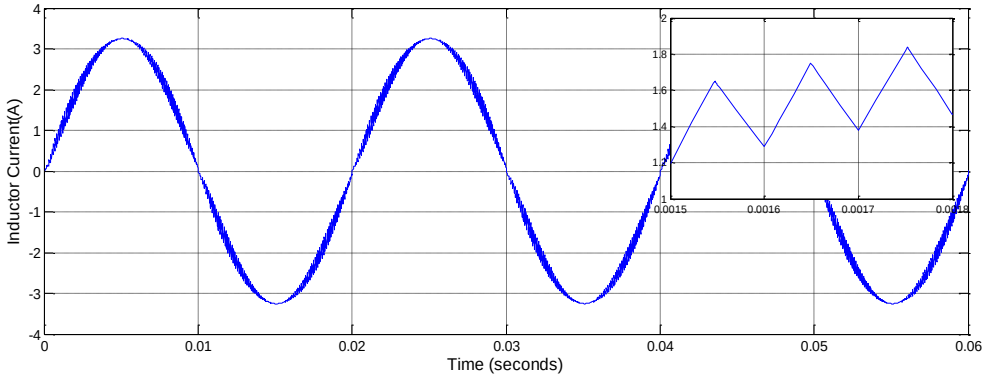

Figure.4.8(c) Inductor current of Novel FSILI

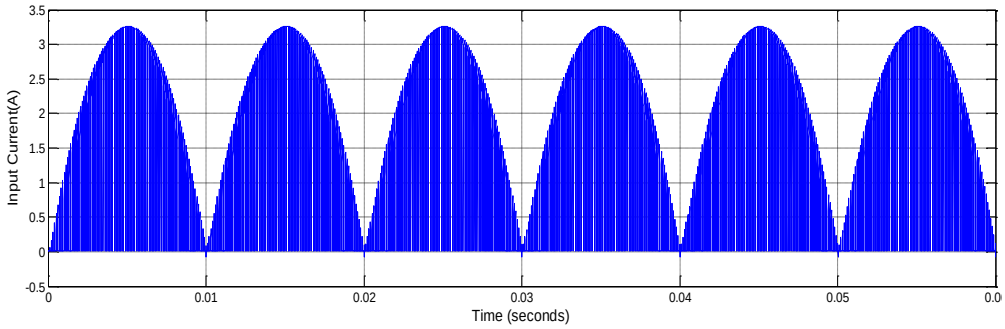

Figure.4.8. (d) Input current of Novel FSILI

Output voltage obtained (Figure. 4.8(a) is a pure sinusoid with very low distortions. Maximum value of the output voltage is the input DC voltage itself. For the resistive load, current through the load (Figure. 4.8(b)) is also simulated. The current is in phase with the voltage and harmonics are very less. Figure.4.8(c) shows inductor current. The maximum inductor current ripple is found to be present at 30^0 as given in the analysis. Zoomed view of inductor current is shown in the inset. The input current (Figure. 4.8(d)) is a fully rectified sine wave which is discontinuous in nature.

For analyzing the harmonic content in the output of proposed inerter, FFT analysis of output voltage and current for both R and RL carried out. The inductance value chosen is 1mH. The frequency spectrum of output voltage(R load) (Figure.4.9) gives a THD of 0.53%. The current THD (Figure.4.10) is also .53% for the given parameters. To understand the reliability of the inverter, RL load is applied and whose frequency spectrum is given in Figure.4.11 and Figure.4.12. The voltage THD is 0.58% and the

current THD is 0.52%. Table 4.2 shows the THD comparison of conventional ILI and Novel FSILI. It can be seen that the THD of the proposed FSILI is near to 0.5% and which is very low in comparison with the case of conventional ILI. So, along with the reduction in number of switches, the quality of output is improved in Novel FSILI topology.

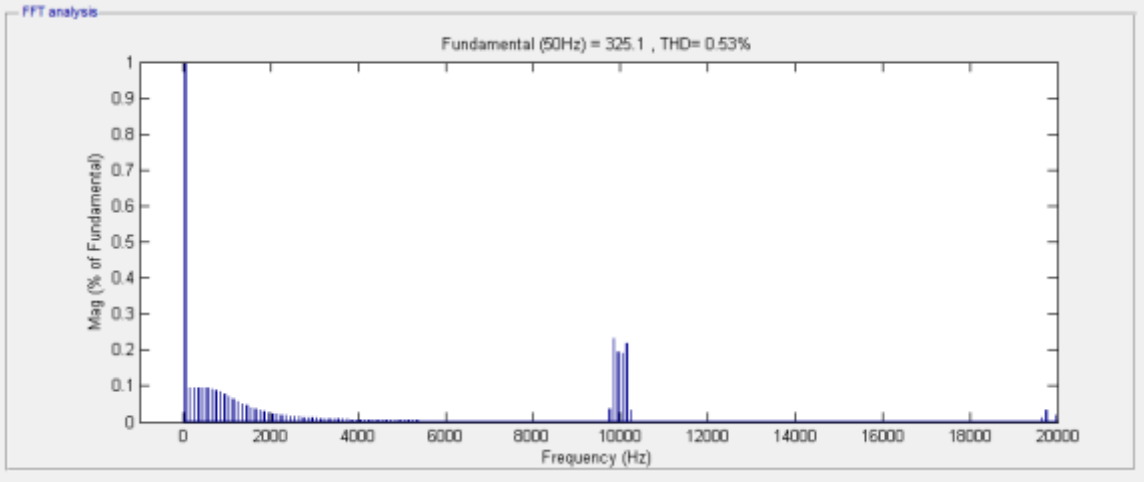

Figure.4.9. Frequency spectrum of output voltage using FFT analysis (R load)

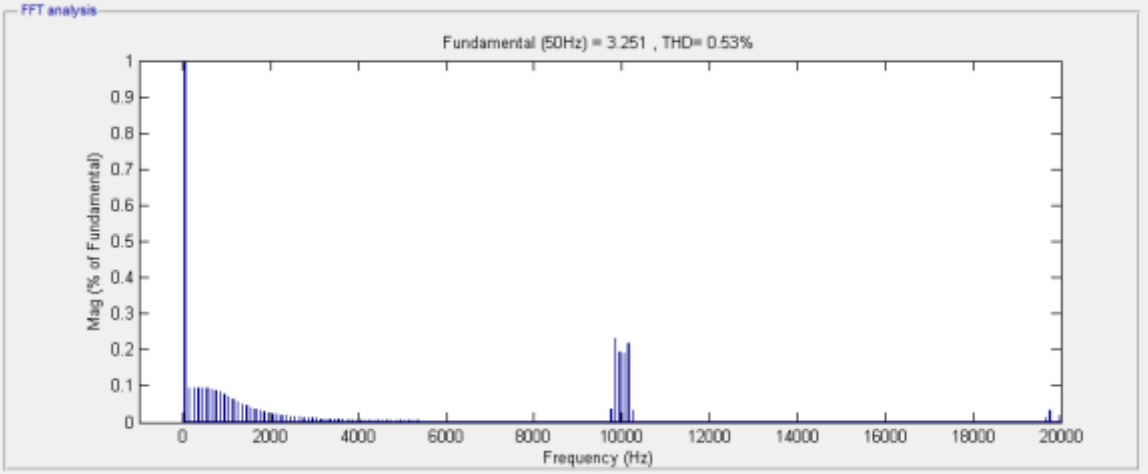

Figure.4.10. Frequency spectrum of output current using FFT analysis (R load)

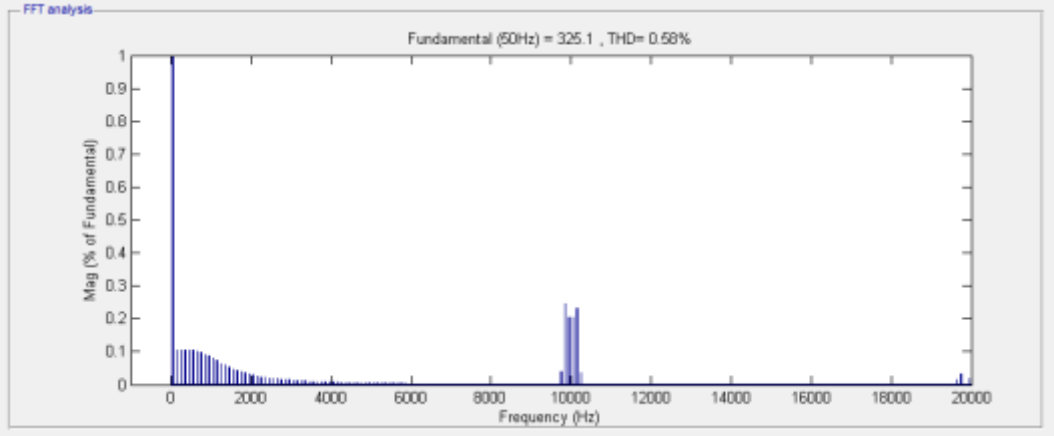

Figure.4.11. Frequency spectrum of output voltage using FFT analysis (RL load)

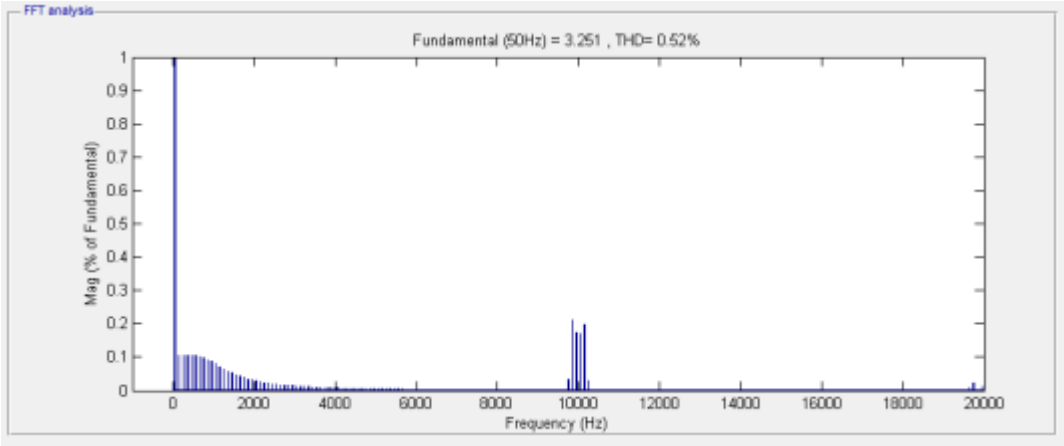

Figure.4.12. Frequency spectrum of output current using FFT analysis (RL load)

Table.4.2. Comparison of THD of Conventional ILI and FSILI

Output Quantity	**Conventional ILI**		**Proposed FSILI**	
	R load	**RL load**	**R load**	**RL load**
%Voltage THD	1.59	1.66	0.53	0.58
%Current THD	1.59	1.69	0.53	0.52

4.5.2. Closed loop Simulation of FSILI

RMS value of actual output voltage is compared with reference value to investigate the controller performance. To analyze the transient response capability, the line regulation, load regulation and reference regulation is carried out. Figure.4.13 shows the simulink model for the closed loop operation under line voltage variation.

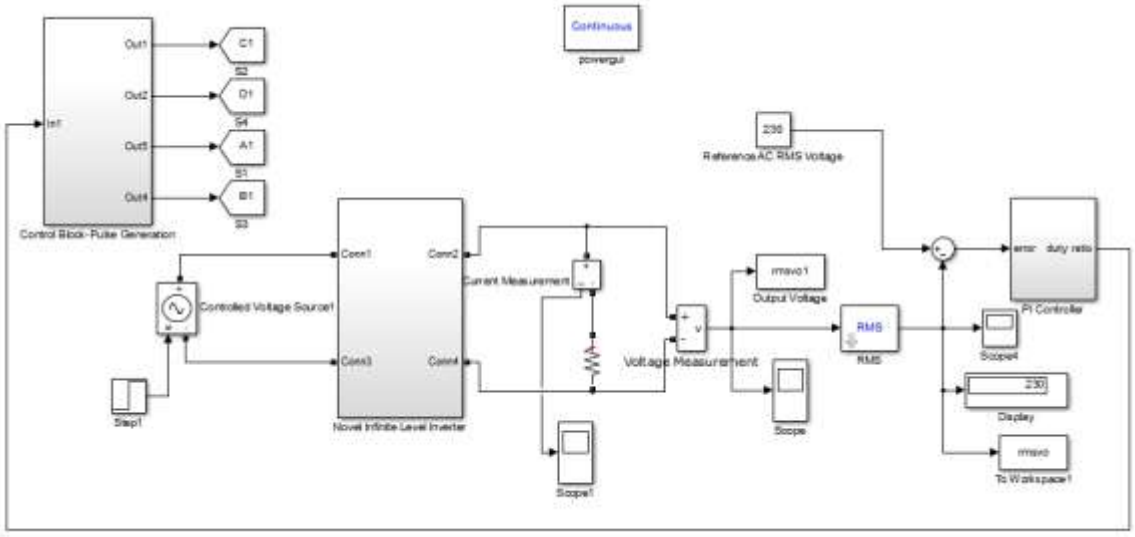

Figure.4.13.Simulink Model for closed loop operation of the NFILI

Line Regulation

To analyze the line regulation, the simulation is carried out with variation in input DC voltage from 325V to 370V at 0.3sec. .The reference voltage is set as $230V_{rms}$. Figure 4.14 shows the actual RMS output voltage along with reference and input voltage. It can be seen that the output voltage settles to 230V (RMS). The Instantaneous output voltage is given in Figure.4.15, which settles at 325 V (max. value).

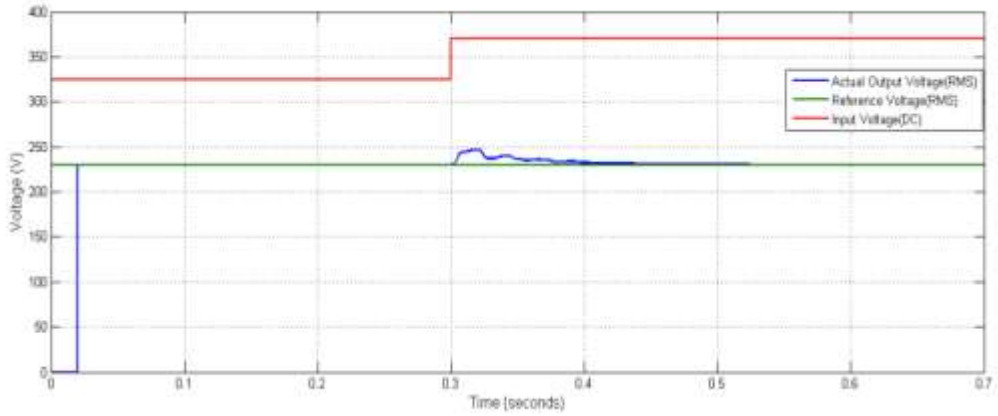

Figure.4.14. Line regulation -tracking of output voltage with reference value

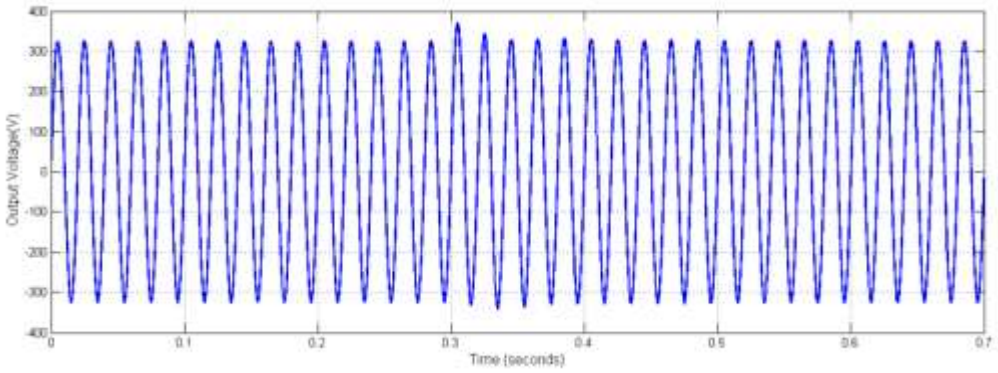

Figure.4.15. Instantaneous output voltage under input voltage variation at 0.3 sec.

Load Regulation

Load is varied from 150 Ω to 150/2 Ω and 150/3 Ω at .25s and 0.5s respectively and the corresponding output voltage variation is observed. Output voltage is obtained to be constant at $230V_{rms}$ (reference voltage) under load variation also. Figure.4. 16 shows the output voltage (rms) for load regulation. Figure.4.17 depicts the instantaneous output voltage under the transient load variation.

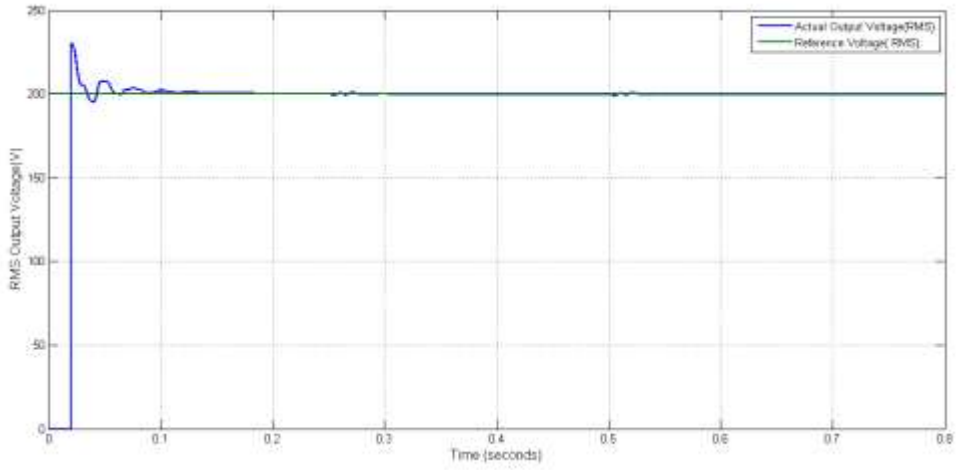

Figure.4.16. RMS output voltage under load variation at 0.25sec. &0.5 sec

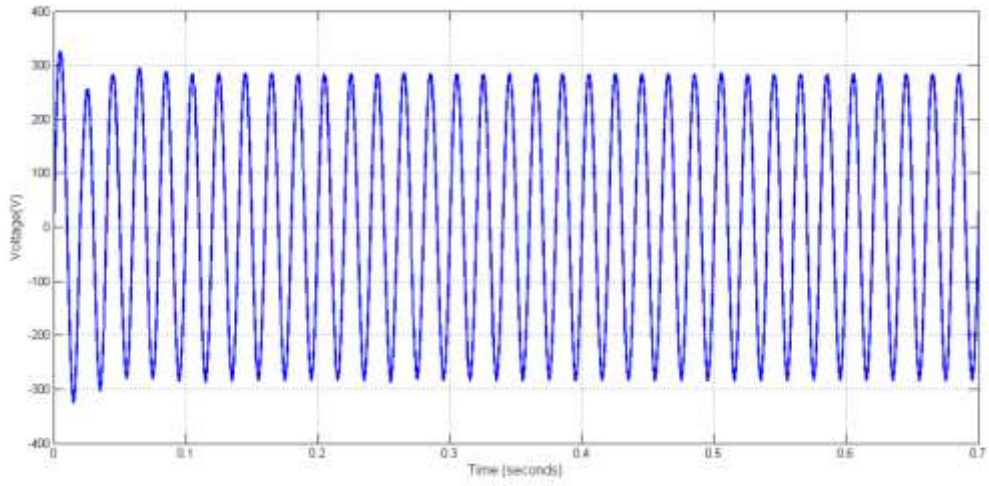

Figure.4.17.Instantaneous closed loop output voltage under load variation at 0.25 sec. and 0.5 sec.

Reference Source Regulation

To investigate the reference regulation performance, the reference voltage RMS is varied from 150V to 200V at 0.3 sec. Transition of reference voltage from $150V_{rms}$ to $200V_{rms}$ is effectively tracked by the inverter at steady state. Figure.4.18 shows the controller tracking with transient change in reference voltage. Steady state error is found to be within the limits. Figure.4.19 shows the instantaneous output voltage corresponding

to the transient change in reference voltage. The output voltage settles to the corresponding peak values (212.13V & 325V).

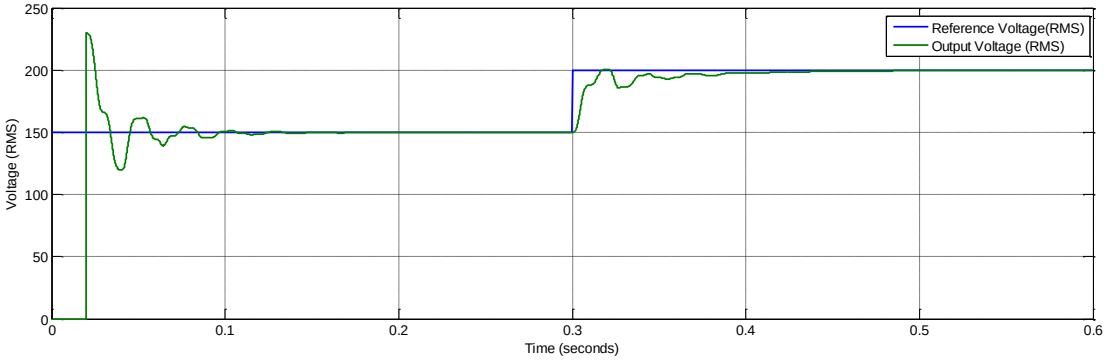

Figure.4.18. Output voltage tracking with variation in reference voltage (RMS)

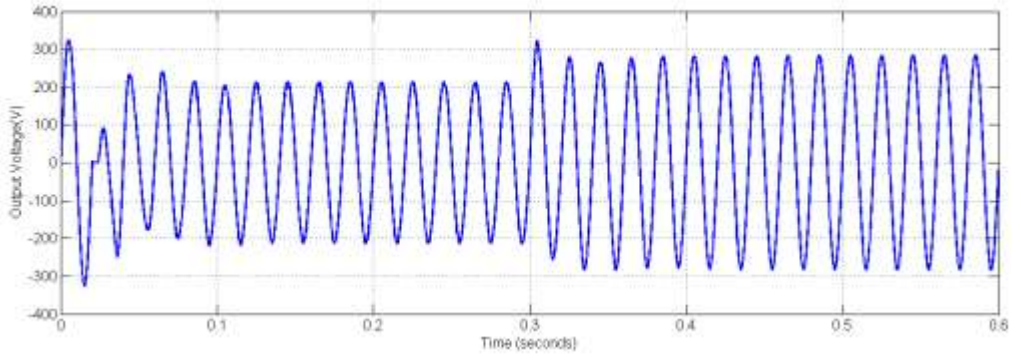

Figure.4.19. Output voltage tracking with variation in reference voltage (Instantaneous value)

From the three closed loop simulation study carried out it can be concluded that the proposed FSILI operates satisfactorily with the disturbances in load, line and reference parameters. The closed loop system is robust and can be implemented in practical applications.

4.6. Summary

Novel Four Switch Infinite Level Inverter with reduced number of switches and low distortion output is proposed in this chapter. The proposed topology gives better output compared to multilevel inverters. Two separate buck circuits are in operation

whose high frequency switches are sine modulated. No unfolding of buck output required here which eliminates the zero crossing ripples. The circuit is less bulky with single inductor and control is very simple. Theoretical concepts were successfully analyzed and verified with the simulation results. THD of the proposed topology is well within the IEEE limits and are very less compared to the conventional ILI topology. Both open loop and closed loop control of the proposed FSILI is done to evaluate the robustness and reliability. The topology can be used in drive applications, renewable power extraction and grid integration, series and parallel compensation of grid etc. The proposed single phase topology can be extended to three phase and which will have high DC bus utilization along with high quality output. In the next chapter, proposed novel three phase infinite level inverter is discussed.

Chapter 5

Novel Three Phase Infinite Level Inverter Topology

5.1. Introduction

In this chapter the three phase modification of the proposed four switch infinite level inverter is discussed. Improved DC bus utilization, reduced switch count are the main features of the proposed inverter. Since only one capacitor and one inductor are present per phase, the weight and cost are less and no need for additional filtering. Magnetic utilization is the maximum since one inductor is in operation in both the half cycles. Control is very simple with the modified PWM technique. DC bus utilization of the proposed three phase inverter is high, compared to voltage source inverter with various PWM techniques, making it more suitable for applications with low input voltage energy sources. The switches are modulated with sinusoidal duty ratio pulses with the intention of getting different voltage levels as the duty ratio is varied. Number of levels in the output voltage depends upon the switching frequency. As the switching frequency is very high compared to fundamental frequency, the output can be considered to have infinite levels and hence the name infinite level inverter. In comparison with conventional three phase ILI topology, the number of switches is less for the proposed three phase ILI. Also, the quality of output obtained is better here. Proposed inverter can be used in drive applications, reactive power compensation of three phase supply systems, for extracting power from renewable sources, in UPS applications etc. Proposed novel three phase infinite level inverter is analyzed, simulated for R load, RL load and motor load.

The chapter is divided into different sections. In section 5.2, the circuit diagram and features of proposed three phase ILI is explained. Analysis of the proposed three phase ILI is done in section 5.3. Both sine PWM and 3rd harmonic injection PWM is considered for analysis. Section 5.4 explains the novel three phase ILI fed induction motor drive. In section 5.5, the simulation study done on the proposed three phase ILI with R, RL and

motor load is explained. The results obtained are analyzed and comparison with the conventional ILI is done. Section.5.6. summarizes the chapter.

5.2. Proposed Three Phase Infinite Level Inverter

From the conventional ILI topology it can be understood that high DC bus utilization with reduced switching losses and minimal conduction loss are some of the desirable features of the inverter used in the medium voltage level. To reduce the switching stress in this voltage ranges, multilevel inverters are used extensively. But MLI will have more number of switches and sources as the output voltage level increases. A novel ILI topology explained in the previous chapter overcomes the demerits of MLI and conventional ILI. The FSILI topology is explained in detail in the previous chapter. The topology can be extended to three phase to achieve high power handling capability with reduced DC bus utilization. All the features in the single phase will be kept intact in this modified Three Phase ILI.

Figure.5.1. shows the proposed three phase ILI topology which is derived from the Novel SILI. Along with the quality AC output obtained, high DC bus utilization makes the proposed topology an alternative to many of the conventional MLI and other inverter topologies.

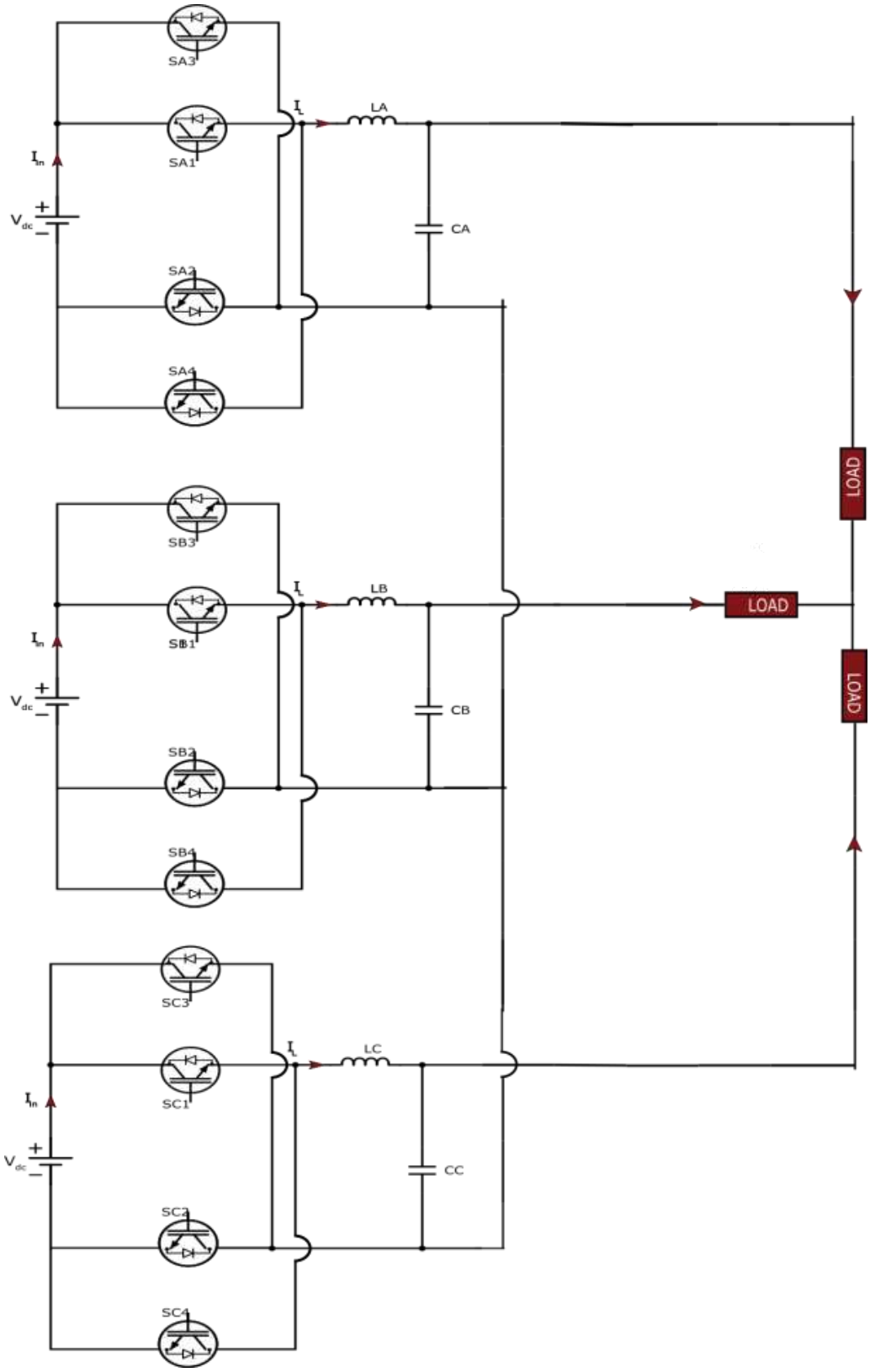

Figure.5.1.Novel three phase infinite level inverter with resistive load

5.3. Analysis of Proposed Three Phase ILI

In this section analysis of the proposed three phase infinite level inverter is carried out. The improvement in the DC bus utilization is explained with sinusoidal PWM modulation and Third harmonic injection PWM. The inverter can be fed from isolated DC sources or isolation can be provided in the load side to avoid short circuit. The modes of operation of the proposed three phase inverter can be explained considering any of the phases. The analysis is same as done in chapter3 section 4.2.3.Since effectively only one switch per phase is operated with high frequency modulation, the switching loss will be low. DC bus utilization of proposed three phase ILI is same as that of conventional ILI. With 3rd harmonic injection PWM, the DC bus utilization is improved.

5.3.1. Analysis with Sine PWM Modulation

Let d_a, d_b & d_c be the duty ratios of PWM pulses for A phase, B phase &C phase respectively.

Since sine PWM is applied we can write for the three phase system,

$$d_a = D_a sin\omega t \tag{5.1}$$

$$d_b = D_b \sin(\omega t - \frac{2\pi}{3}) \tag{5.2}$$

$$d_c = D_c \sin(\omega t + \frac{2\pi}{3}) \tag{5.3}$$

By applying the above duty ratio command to the three basic inverter units we can obtain the phase voltages as,

$$V_a = d_a V_{dc} \tag{5.4}$$

Since DC input will be equal to the maximum value of output, we can write, $V_{dc} = V_m$ and substituting for d_a from (7), (10) becomes,

$$V_a = D_a V_m Sin\omega t \tag{5.6}$$

$$V_b = D_b V_m Sin(\omega t - \frac{2\pi}{3}) \tag{5.7}$$

$$V_c = D_c V_m Sin(\omega t + \frac{2\pi}{3}) \tag{5.8}$$

For a balanced three phase system, the duty ratios D_a, D_b & D_c should be equal which is given by D.

So, the line voltages can be represented as,

$$V_{ab} = \sqrt{3}DV_m Sin(\omega t + \frac{\pi}{6}) \quad (5.9)$$

$$V_{bc} = \sqrt{3}DV_m Sin(\omega t - \frac{\pi}{2}) \quad (5.10)$$

$$V_{ca} = \sqrt{3}DV_m Sin(\omega t + \frac{5\pi}{6}) \quad (5.11)$$

So the peak value of output voltage is given by

$V_{peak} = \sqrt{3}DV_m$

Taking $D = 1$,

$V_{peakl} = \sqrt{3}V_m$

$$V_{rmsl} = 1.23V_{dc} \quad (5.12)$$

So the DC bus utilization is high compared with Sine PWM VSI and SVPWM VSI. For obtaining a line –line RMS voltage of 400V only 325V DC is to be applied.

5.3.2. Third Harmonic Injection PWM Applied to Proposed Three Phase ILI

Proposed Inverter can be modulated with third harmonic Injection PWM method, which is an approximate implementation technique for SVPWM. By this method, the DC bus utilization can be further improved. Figure 5.2.shows the third harmonic injected modulating signal employed in the inverter control.

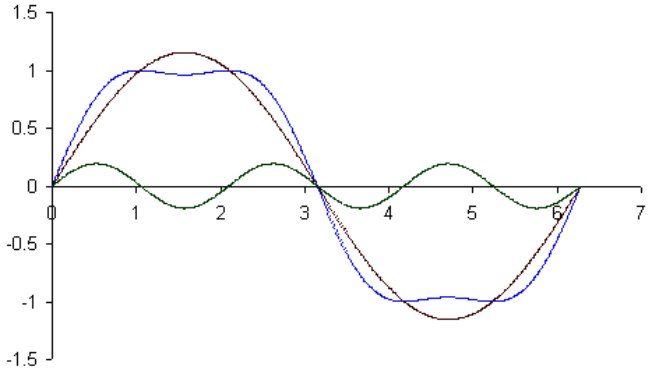

Figure.5.2. Third Harmonic Injection PWM technique

Modulating signal for third harmonic injection PWM technique is given by

$$d = DSin\omega t + KSin(3wt) \tag{5.13}$$

For optimum condition it is given as D=2⁄√3 and K=1⁄6K = $^1/_6$ so that the reference signal is obtained as

$$d_a = 1.1547sin\omega t + 1/6Sin(3wt) \tag{5.14}$$

Similarly other phase reference signals can be represented with corresponding phase displacements. Main advantage of third harmonic injection PWM is that the output line voltage fundamental amplitude will increase by 15.4%. This will effectively improve the DC bus utilisation.

For the proposed modified three phase infinite level inverter with 3rd Harmonic Injection PWM, only 282V is required to get 400V (RMS) in the line voltage.

So,

$V_{rmsl} = 1.42V_s$

Bar diagram shown in Figure 5.3 represents the comparison of DC bus voltage required by different inverter topologies applied with various modulation strategies. The Novel Three phase infinite level inverter requires only 325V to obtain 400V (RMS) in the line voltage. With Third harmonic injection PWM technique, the DC voltage requirement further reduced and only 282V is required to obtain the given line voltage. Figure 5.4

shows the comparison of the DC bus utilization of VSI, VSI with sine PWM, VSI with space vector PWM (third harmonic injection PWM), conventional TILI with sine PWM, Proposed novel TILI with sine PWM and Proposed novel TILI with space vector PWM. The DC bus utilization is highest for proposed TILI with third harmonic injection PWM.

Thus, it can be seen that the proposed topology has least DC bus requirement same as conventional TILI, with an additional benefit of reduction in switch count.

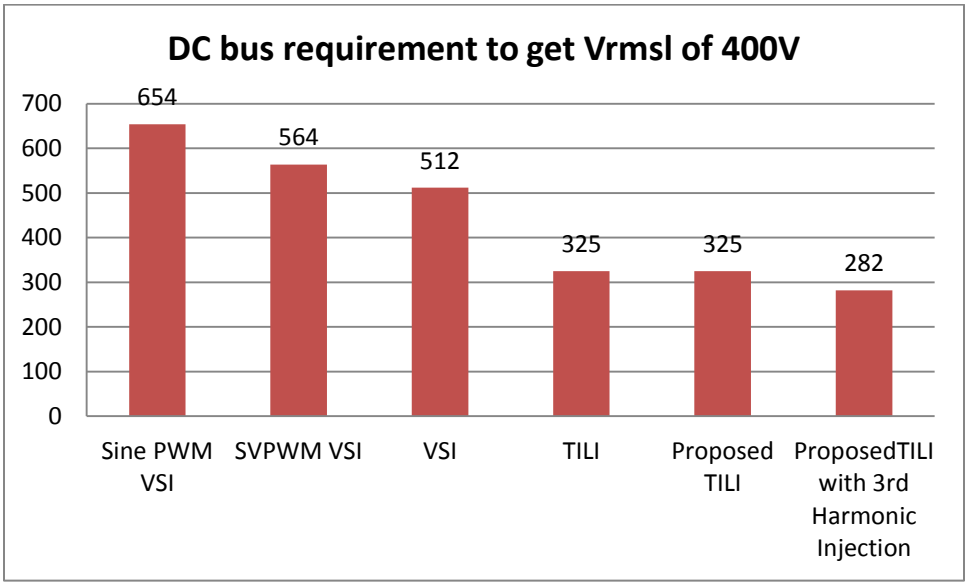

Figure.5.3. Comparison of DC bus voltage required to get $400V_{l(rms)}$

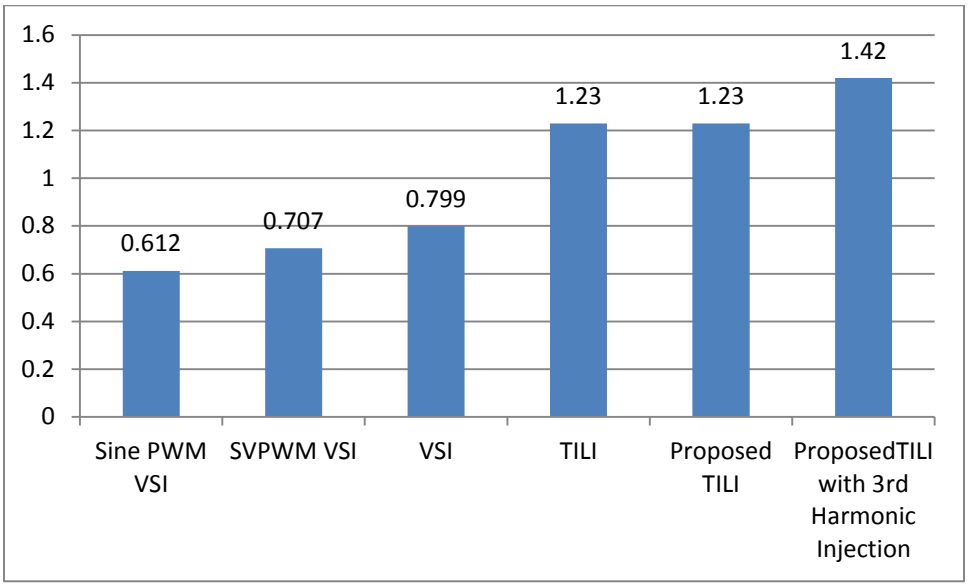

Figure.5.4. Comparison of DC bus utilization of various inerter topologies

5.4. Novel Three Phase ILI Fed Induction Motor Drive

Proposed novel three phase infinite level inverter can be used in drive applications. Improved DC bus utilization of the proposed topology along with the low distortion output enables the satisfactory operation when connected to motor load. Torque pulsation will be less due to smooth nature of output. Open ended winding induction motor is considered here since each phase can be separately excited with corresponding inverters. Figure .5.5. shows the circuit diagram of NTILI fed three phase induction motor drive.

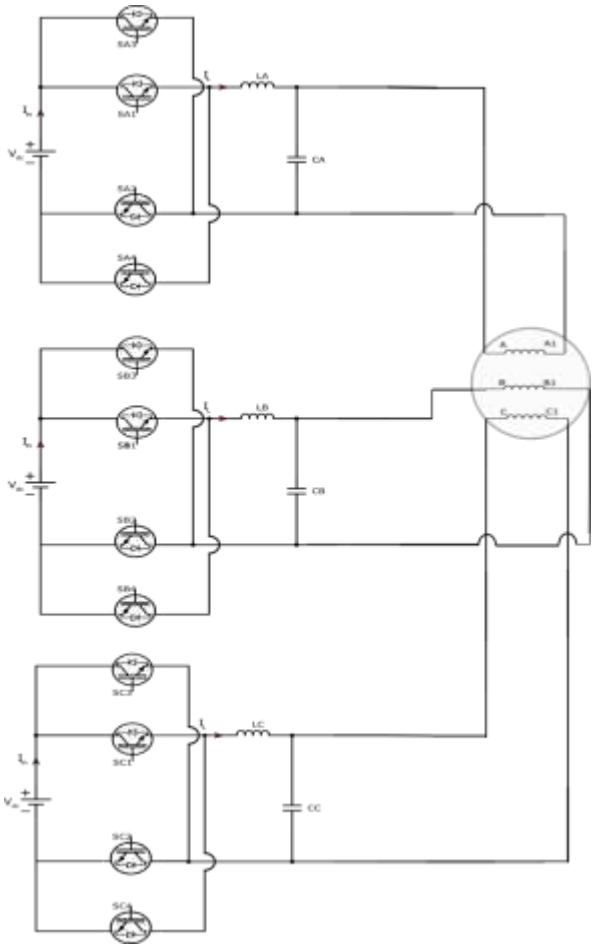

Figure.5.5.Novel three phase infinite level inverter fed induction motor drive

5.5. Simulation of Novel Three Phase Infinite Level Inverter

In this section, simulation of proposed novel three phase infinite level inverter under different load conditions is carried out. The proposed topology is given with resistive load, RL load and motor load for simulation purpose. Phase voltage, line voltage and phase current with proposed sine PWM and Third harmonic injection PWM is obtained. FFT analysis is carried out with R load and RL load and the results are compared.

5.5.1. Simulation of Novel TILI with R load and RL load

The simulation of novel three phase inverter is carried out with resistive load and RL load. Table5.1. List the parameters used for the simulation. The load is balanced with star connection.

Table 5.1 Simulation Parameters of Novel Three Phase ILI

Parameters	***Values***
Input Voltage, Vs	325V
Inductor, L	20mH
Capacitor, C	.6μF
Switching Frequency, fs	10kHz
Load Resistance, R(Three phase balanced star connected load)	100Ω/phase
Inductance for RL load(Three phase balanced)	1mH

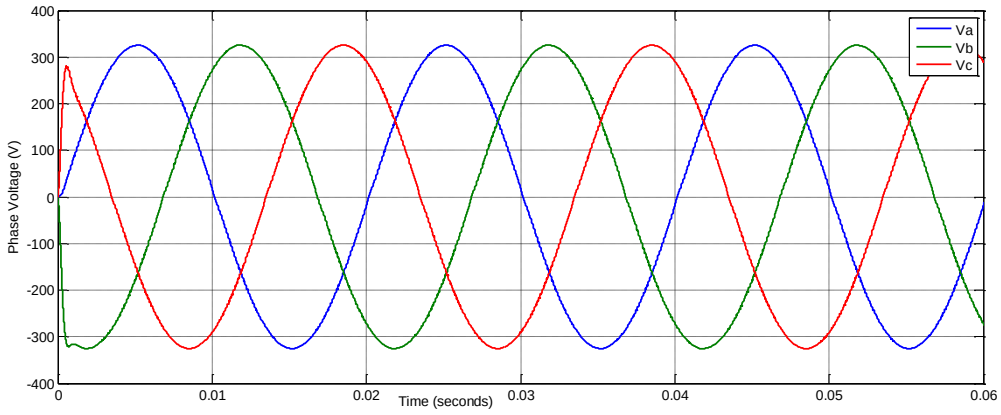

Figure.5.6. Phase voltage waveform of proposed three phase ILI

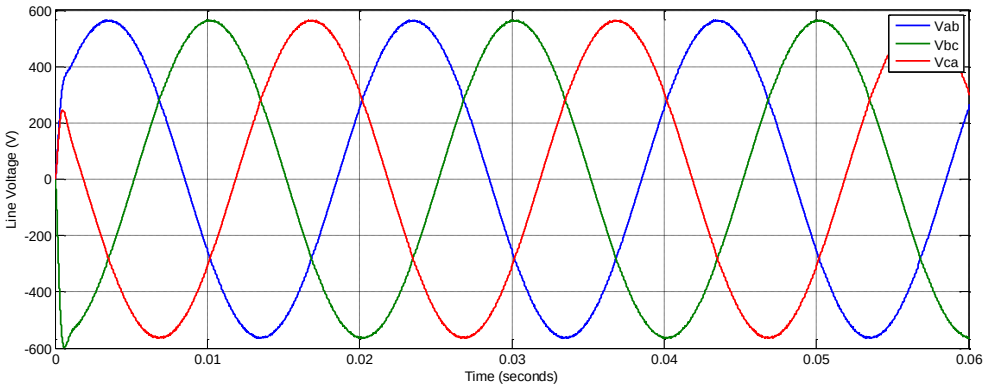

Figure.5.7. Line voltage waveform of proposed three phase ILI

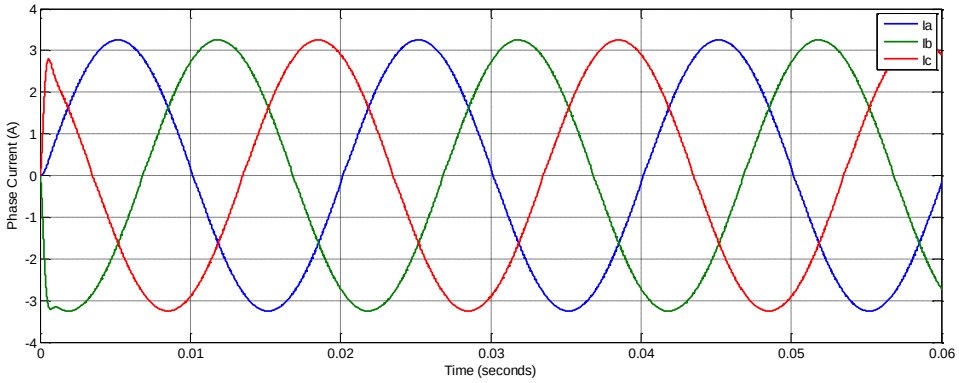

Figure.5.8. Phase current waveform of proposed three phase ILI

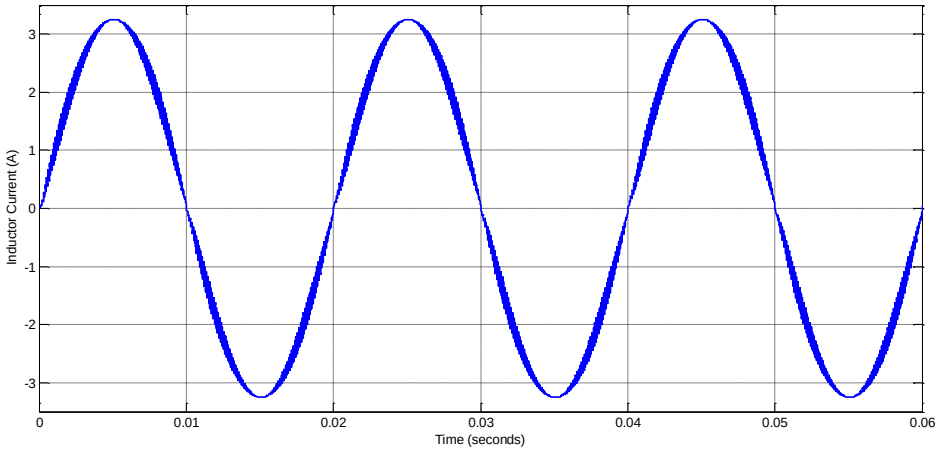

Figure.5.9. Inductor current waveform of proposed three phase ILI

Simulation of the proposed novel three phase ILI is carried out with R load and the results are obtained as given in Figure 5.6 to Figure 5.9. Phase voltage obtained (Figure 5.6) is having the peak value as the input DC voltage given by 325V. Corresponding RMS value is 230V (Approx.). Line voltage (Figure 5.7) waveform has the peak value 565V, corresponding RMS value is 400V (Approx.) For a resistive load of 100Ω, the phase current obtained is shown in Figure 5.8. Inductor current waveform is given in Figure 5.9 and it can be seen that the inductor current is having ripples corresponding to charging and discharging in the respective operating modes.

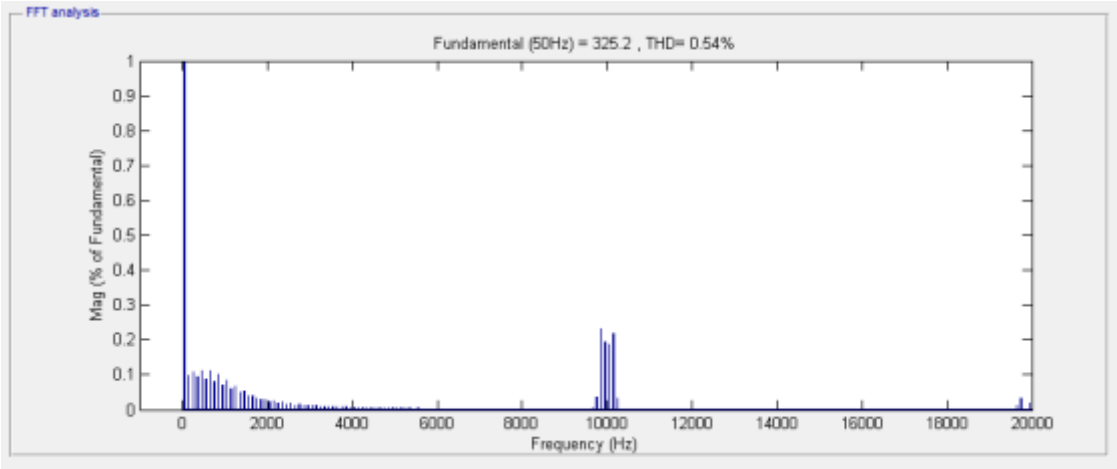

Figure.5.10. FFT analysis of output phase voltage (R load)

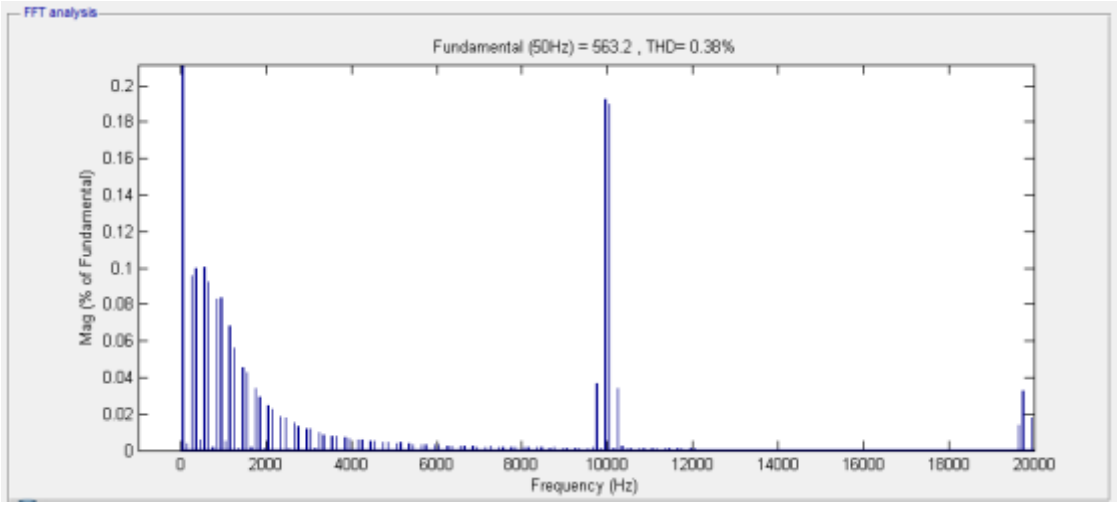

Figure.5.11. FFT analysis of output line voltage (R load)

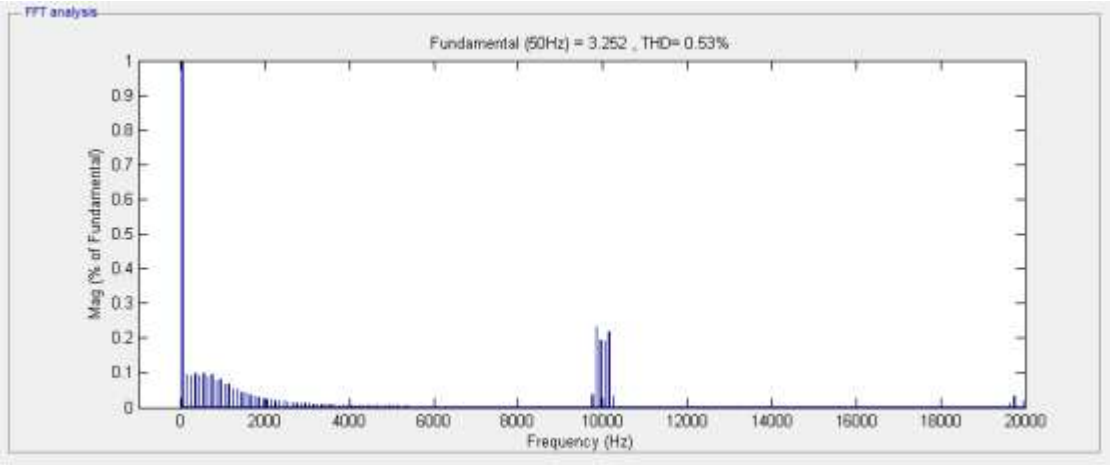

Figure.5.12. FFT analysis of output phase current (R load)

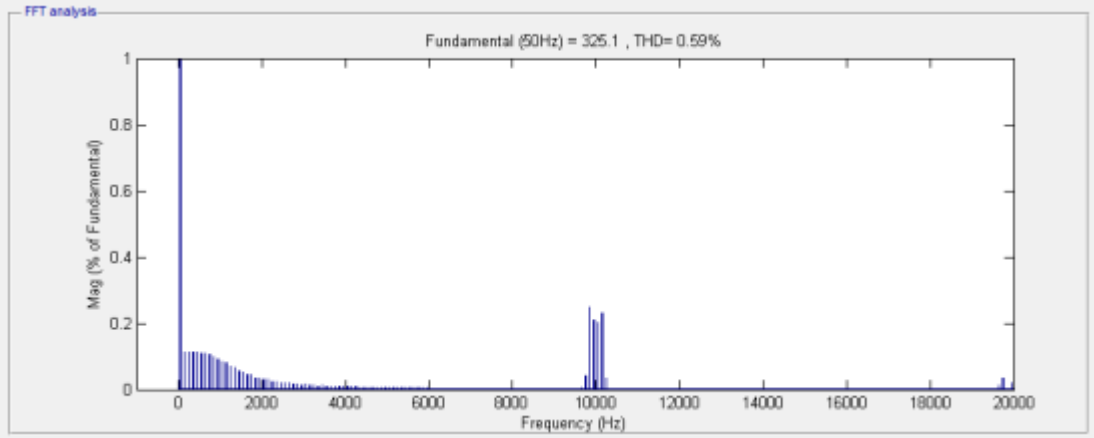

Figure.5.13. FFT analysis of output phase voltage (RL load)

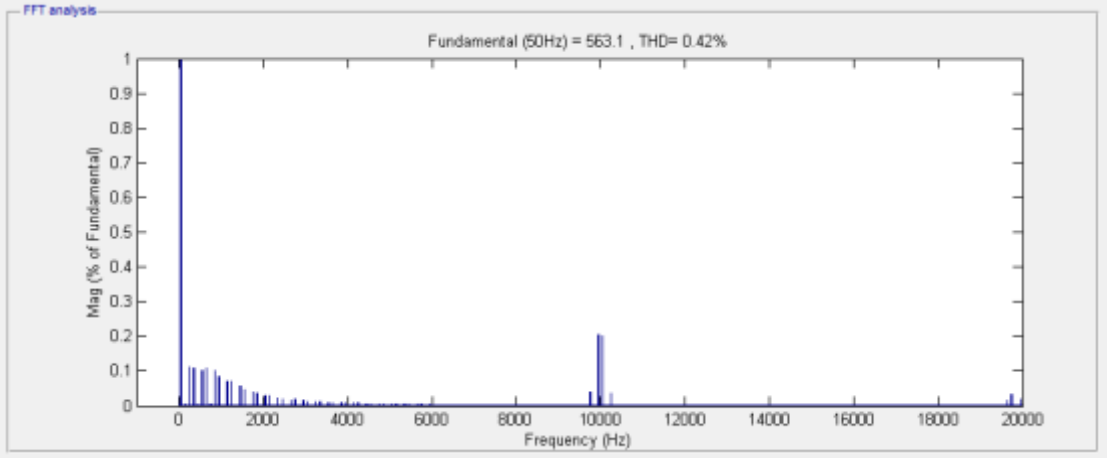

Figure.5.14. FFT analysis of output line voltage (RL load)

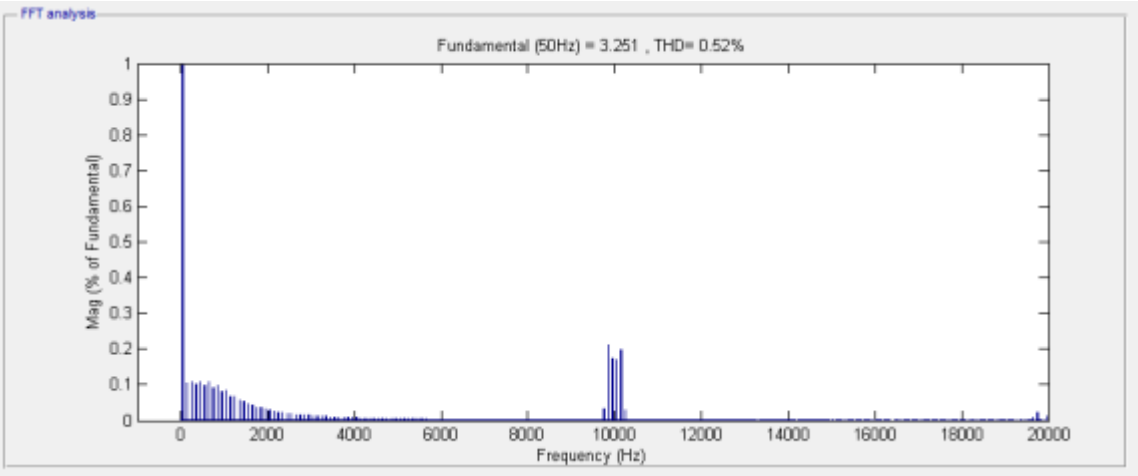

Figure.5.15. FFT analysis of output phase current (RL load)

FFT analysis is carried out both for restive load and RL load. Figure 5.10.shows the harmonic spectrum corresponding to phase voltage of the proposed three phase ILI. THD is found to be 0.54%. THD of the line voltage (Figure5.11.) is 0.38% and phase current THD is 0.53%. (Figure.5.12.).

Similar analysis is done with RL load and corresponding frequency spectrums are obtained. Figure 5.13.shows the harmonic spectrum of phase voltage and the THD is obtained as 0.59%. THD of line voltage is given in Figure 5.14 which is 0.42%. Phase current THD is 0.52% as given in Figure5.15.

Table 5.3 gives the comparison of THD of proposed three phase ILI with conventional ILI topology. THD obtained with R load and RL load re compared. It can be concluded that under various load conditions the THD obtained for proposed three phase ILI is far less than that of conventional ILI .and is near to 0.5%. The value is well within the IEEE 519 standards and practical implementation will very much satisfy the load requirements.

Table 5.2 THD comparison of proposed TILI with Conventional TILI under R and RL load

Output Quantity	Conventional TILI(% THD)		Proposed TILI (%THD)	
	R load	**RL load**	**R load**	**RL load**
Line Voltage	1.29	1.36	0.38	0.42
Phase Voltage	1.59	1.66	0.54	0.59
Phase Current	1.59	1.59	0.53	0.52

Proposed three phase infinite level inverter is simulated with third harmonic injected PWM. With 3rd harmonic injection PWM, the DC bus utilization is improved. Line voltage waveform is shown in Figure. 5.16. Frequency spectrum of line voltage for the 3rd harmonic injection PWM is given in Figure 5.17. THD obtained is high compared with sine PWM modulation.

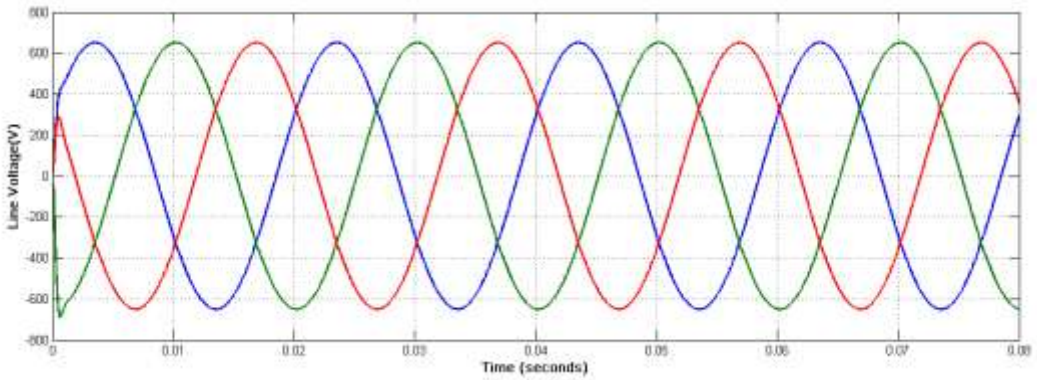

Figure.5.16. Line voltage with third harmonic injection PWM

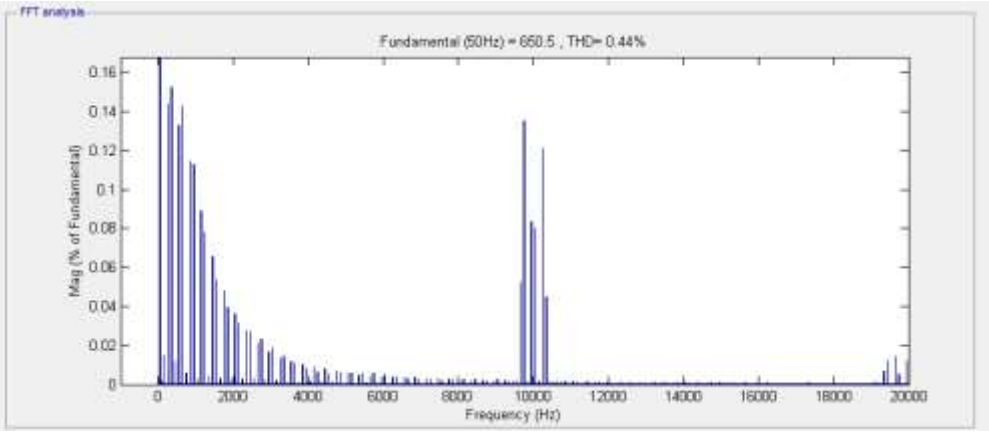

Figure.5.17. FFT analysis of line voltage with third harmonic injection PWM

Maximum value of output voltage is 650.5V .for an input DC voltage of 325V. There is large increase in the DC bus utilization with this third harmonic injection PWM but the THD is high compared with sine PWM. Line voltage THD obtained is 0.44%. Increase in THD is due to the injection of additional third harmonic component.

5.5.2. Simulation of Novel Three Phase ILI Fed Induction Motor Drive

To investigate the performance of the novel infinite level inverter, the inverter is used to drive a three phase induction motor. The parameters of the open ended induction motor are given in Table 5.3. Since the Novel infinite level inverter is capable of supplying quality AC output with minimal DC bus voltage, this can be used in the application where the DC link voltage is less with a need for ripple less output. The simulation is carried out in Matlab/Simulink with the Plexim toolbox for incorporating the open ended winding induction motor

Table.5.3. Motor Parameters

Parameters	***Values***
Power (kW)	1.1 kW
Voltage (V)	415V
Rated Current (A)	2.77A
Frequency (Hz)	50 Hz
Rated speed (rpm)	1415 rpm

Figure.5.18. and Figure 5.19.shows the simulation results of induction motor fed from the proposed three phase ILI. The open loop speed response and torque response is shown. Also, the phase voltage and current waveforms are depicted.

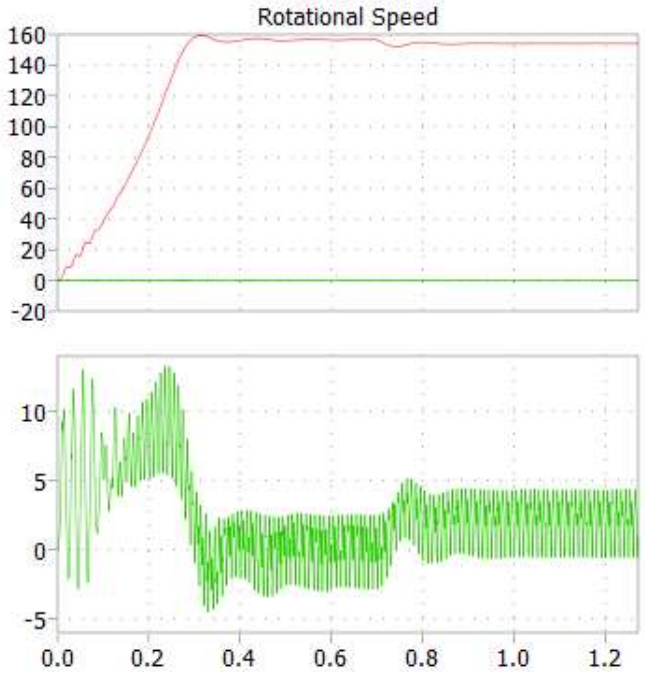

Figure.5.18. Speed and torque response of the proposed three phase ILI fed Induction Motor

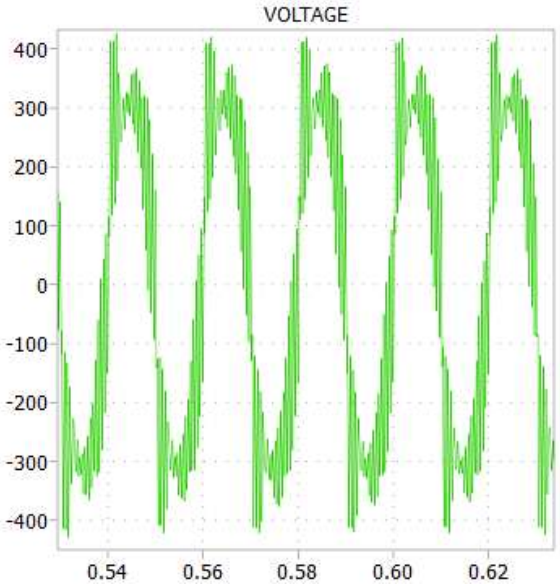

Fig.5.19. Phase voltage of proposed three phase ILI fed Induction Motor drive.

Drive performance of the proposed three phase infinite level inverter is validated from the simulation results. Any type of closed loop control like V/f control and vector control can be used for improved performance.

5.6. Summary

In this chapter a novel three phase inverter derived from a novel four switch infinite level inverter is described. Proposed inverter has less number of switches and passive elements compared to conventional MLI and ILI. DC bus utilization is very high compared to normal PWM VSI inverter, SPWM inverter and SVPWM modulated inverters. With the help of 3^{rd} harmonic injected PWM, DC bus utilization is further improved. THD of the output voltage is obtained to be very less for the given parameters. Drive performance of the proposed inverter is validated with the simulation of proposed three phase ILI fed induction motor drive. Proposed three phase infinite level inverter with its low THD and high DC bus utilization can be a possible solution for various industrial applications. It can also be used in series and parallel grid compensation applications. In the next chapter, the grid control and integration of the proposed FSILI is discussed.

Chapter 6

Grid Tied Operation of Proposed Four Switch Infinite Level Inverter

6.1. Introduction

Grid Integration of novel four switch infinite level inverter is discussed in this chapter. High demand for energy accelerated the research in renewable energy systems and the extraction of power from renewable sources. Conventional grid system in India is AC grid and thus extracted power from various renewable sources should be integrated to the AC grid. The distributed generation, which is gaining much popularity these days, essentially requires integration of the produced electricity to grid. STATCOM, DVRs etc. also make use of the gird connected operation of inverters in a different way. Proposed Four Switch Infinite Level Inverter with its distortion free output is a viable solution for power extraction from renewable sources. Power thus extracted should be integrated to the utility grid for the effective utilization. In this chapter a new current control algorithm for the proposed FSILI is discussed. Using this current control technique a grid control technique is established to modulate the power flow to the grid

Section 6.2 explains the basic circuit and features of grid tied FSILI. In section 6.3.Grid power control concept is explained with the single line diagram of grid integration and the control block diagram. In section.6.4 the current control logic applicable to grid integration of proposed FSILI is detailed. The operating modes of current controlled FSILI are explained in section 6.5. The standalone current control operation of the proposed FSILI is given in section 6.6. Section.6.7. explains the simulation work carried out in grid connected mode and islanding mode of operation of FSILI. The chapter is concluded in section 6.8.

6.2. Proposed Grid Tied Four Switch Infinite Level Inverter

A novel four switch grid tied infinite level inverter is explained in this section. Proposed infinite level inverter with the reduced number of switches and passive

elements produces near sinusoidal output. Here output voltage level depends on the switching frequency. Switching frequency is very high so that the output voltage obtained can be said to have infinite level. Using this inverter, power from RES can be extracted efficiently.

Proposed grid tied infinite level inverter is shown in Figure 6.1.Inverter has four switches in which two will operate at high frequency and the other two in the fundamental frequency. For positive and negative half cycles, two separate buck converter operation with sinusoidal modulation is executed. Switched mode operation of the inverter enables reduction of harmonics and with the sinusoidal modulation, harmonics will be almost zero. The switches S_1 & S_3 are operated at high frequency for positive and negative half cycle of the output current respectively. S_2 is ON for the positive output current and S_4 is ON for negative output current. The body diodes of low frequency switches play an important role in the operation of the proposed inverter.

Relationship between input and output voltage can be deduced from the analysis of the inductor current waveform during the charging and discharging modes explained in chapter 4. From the analysis the gain of the inverter is given by

$$d(t) = \frac{v_{cf}(t)}{V_{in}} \tag{6. 1}$$

Where $v_{cf}(t)$ is the voltage across the filter capacitor and V_{in} is the input voltage from renewable energy source.

Where the inductor is designed with the expression

$$L_{min} = V_{cf}\,(\sqrt{2}(V_{in}) - V_{cf}\,)/(2 * \Delta \mathrm{I}_{\max} * f_s * V_{in}) \tag{6. 2}$$

And the filter capacitor value is given by

$$C_{fmin} = \Delta I_{max}\,/(8 f_s\ \Delta V_{cf\,\max}) \tag{6. 3}$$

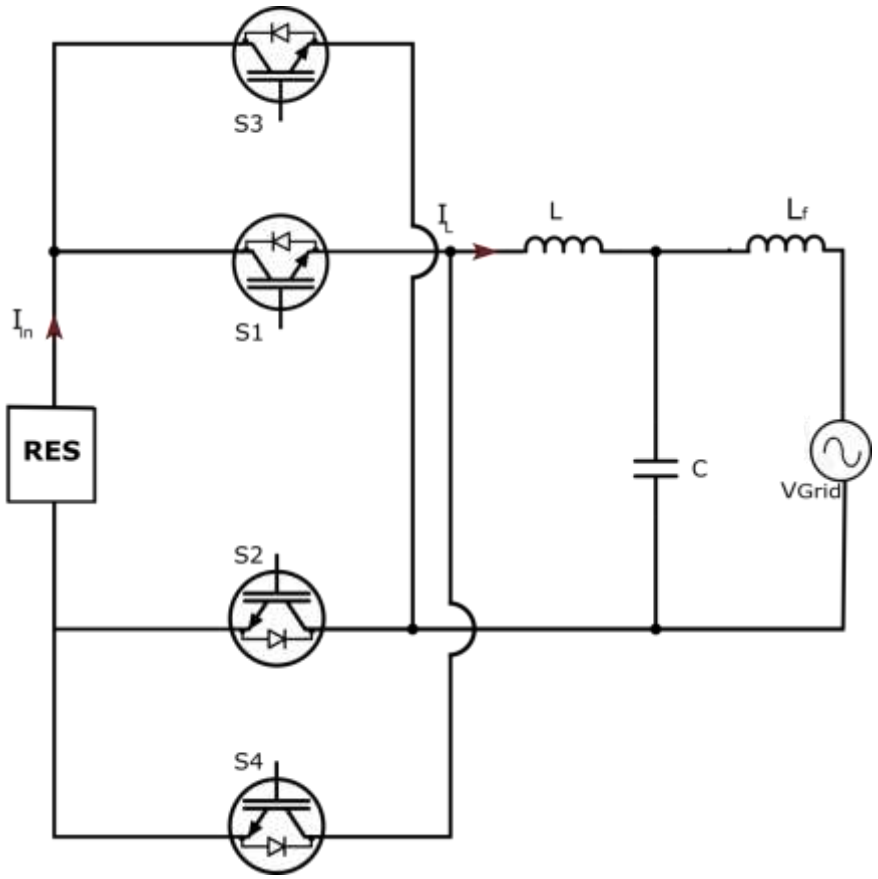

Figure.6.1. Novel Four Switch grid tied infinite level inverter

The topology is an improvement from the conventional ILI topology which has a front end buck converter followed by an H-bridge inverter. In the infinite level inverter explained in chapter 3, there are 5 active switches and one diode present. With the modified inverter arrangement, the switching losses are reduced considerably with an improvement in the output voltage quality. The unfolding ripple which is a distortion present in the conventional ILI is eliminated here with the separate buck circuits.

The FSILI can be operated in the grid connected mode and the islanding mode. In the grid tied operation, it is possible to supply the extracted power from the RES to grid for the effective utilization. The proposed grid control strategy applied in the novel grid tied four switch inverter is discussed in the next section.

6.3. Grid Control of the Proposed FSILI

It is very important to extract the maximum possible power from the RES and to inject on to the grid in a most efficient manner. Using the maximum power point tracking methods, it is possible to extract the power effectively. An efficient grid control method is necessary to inject this extracted power to grid. Phase lock loops (PLL) explained in [88] is used to identify the exact phase of the grid voltage. Many control methods in the literature [84], [85] employ PI, PR and SMC etc. for the grid side control of the inverter. Most of the methods are complex and need extensive control algorithms for implementation. Hysteresis controller [86] based grid integration is very simple and along with power control algorithm it will produce promising results. In the proposed grid tied inverter a hysteresis based current control technique is implemented with a novel grid control method. Here, the unity power factor power injection is ensured.

Output circuit of the proposed four switch grid tied ILI is shown in Figure 6.2. It can be seen that the filter circuit in the output will produce a lag in the grid current but the injected current and the grid voltage will be in phase.

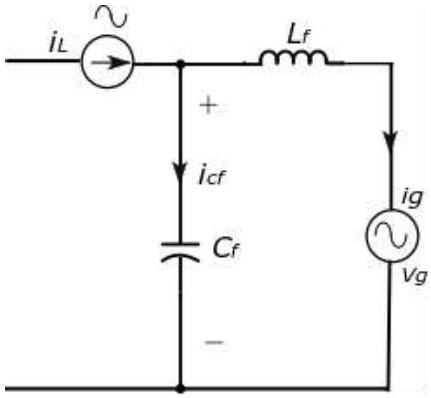

Figure.6.2.Output circuit of proposed grid tied FSILI.

From the grid voltage, the phase angle is detected to ensure a proper injection of power on to grid. For the hysteresis current controller to operate, it is required to have inductor current reference i_L^* which is compared with the actual inductor current i_L to obtain error command for the hysteresis controller. I_L^*, the magnitude of the reference inductor current is obtained from the power to be injected in to grid. In case of MPPT methods,

the active power P_i will be obtained from the MPPT and the Q_i will be given as reference value. Here, the reactive power control is not considered and only active power is injected on to grid, even though both ways are possible. Capacitor voltage $V_{cf}$is sensed and given to the I_L^* calculation block for obtaining the magnitude of reference inductor current.

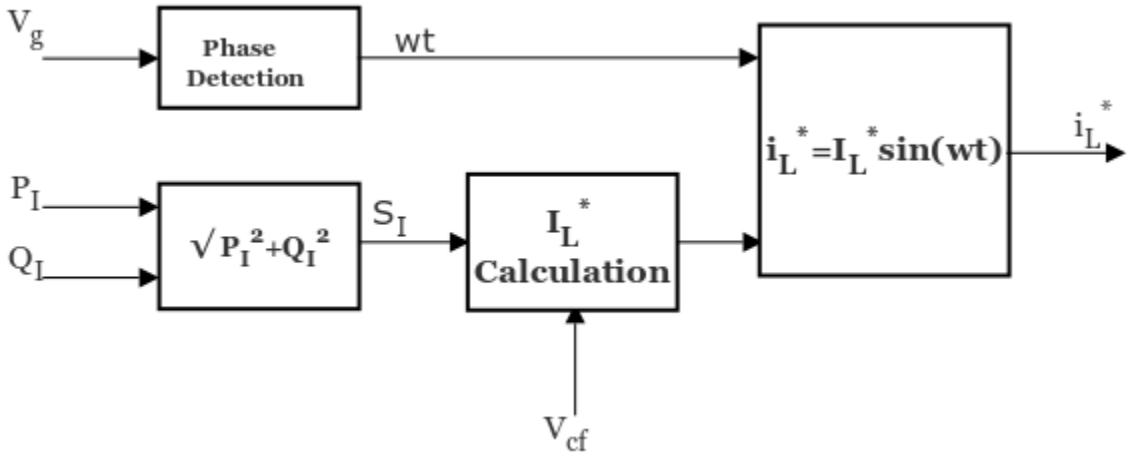

Figure.6.3. Block diagram of proposed power control for grid tied operation.

The apparent power requirement of the grid is resolved in to the voltage magnitude and angle component using the control algorithm. Since unity power factor operation is explained, the reactive power injected is assumed to be zero.

We have, $S = \sqrt{P^2 + Q^2}$ (6.4)

Taking Reactive Power, $Q = 0$,

We can write,

$Apparent\ Power(S) = Active\ Power(P)$

$Apparent\ Power(S) = V_{rms} \times I_{rms}$

$$I_L^* = \sqrt{2} \times \frac{Apparent\ Power(S)}{V_{rms}} \quad (6.5)$$

Using the hysteresis current control method with the obtained I_L^* switching pulses for the inverter is obtained. Current control method implemented is explained in the next section.

6.4. Current Control of Proposed FSILI in Grid Tied Operation.

In voltage control methods using the pulse width modulation techniques, voltage is the control parameter and the current is not considered for the same. In voltage controlled PWM techniques, there can be high frequency switching and filter circuits are essential for obtaining the harmonic free outputs. With the proper design of the hysteresis band, the exact tracking of the actual quantity with reference can be ensured. Also, in grid tied operations, for the control of power to be injected to grid, the current control method is the most suitable method for obtaining distortion free grid current. Here, i_L is compared with i_L^* in the current control loop and high frequency switching pulses are obtained. A resolver circuit will be used to obtain the switching pulses for S_1 and S_3 for positive values of inductor current and negative values of inductor current respectively. Figure.6.4 shows the switching pulse generation block. From the i_L^*, using positive half cycle detector the gate signal for S_2 is obtained. With the help of negative half cycle detector switching pulse for S_4 is resolved.

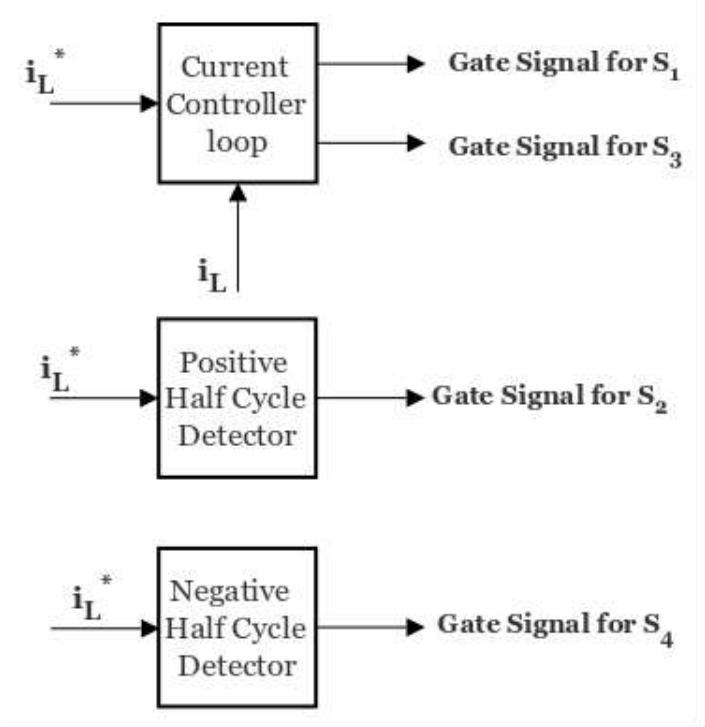

Figure.6.4. Switching pulse generation using the proposed current control technique

6.5. Operating Modes of Current Controlled FSILI

Current controllers used for inverter operation can be ramp comparison controller, predictive controllers and hysteresis controllers. Hysteresis controller is the simplest one to implement and it does not require the knowledge of load parameters. Hysteresis controllers has fast response current loop. Here, for the proposed grid tied FSILI, hysteresis current control method is used due to the advantages it has. Reference inductor current obtained from the power control algorithm is used to compare with the actual inductor current to produce the switching pulses. Error between the two will be given to hysteresis band controller. When the error exceeds the boundary conditions, the switching states will be changed. The low frequency switches which operate at fundamental frequency receive switching pulses from a zero crossing detector whose input is the reference current command.

In the current control of proposed FSILI, there are 4 different modes of operation. For the inductor current greater than zero there can be two modes where as for $i_L^* < 0$ the other

two modes can be explained. Figure.6.5. shows the detailed control block diagram of the current controlled inverter. Various modes of operation are based on the current polarity, which is explained the coming sub sections.

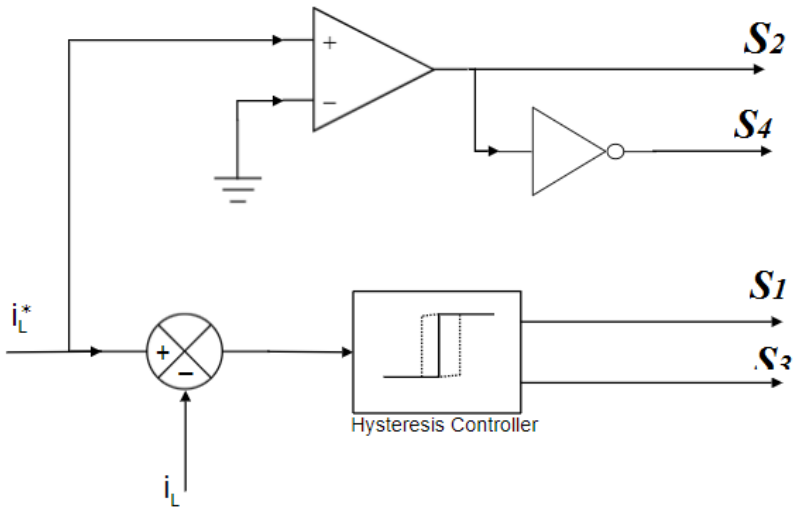

Figure.6.5. Current control scheme for the FSILI

6.5.1. $i_L^* > 0$, Switch S_2 is Always ON

Mode I ($i_l < i_L^* - h$): (S_1 & S_2 ON)

In this mode shown in Figure.6.6.(a), when the error between reference and actual inductor current reaches the lower hysteresis band, the switch S_1 will be turned ON, S_2 remains in the ON condition during the entire positive half cycle. The current will flow to grid from RES through inductors, S_1 & S_2 . The capacitor C_f gets charged.

Mode II ($i_l > i_L^* + h$): (S_1 is OFF, S_2 is ON)

When the current increases till the upper band, to limit the current within the band, S_1 turned OFF, the stored inductor energy will be released through the switchS_2 , the body diode of S_4 and to the grid. The capacitor C_f gets discharged in this mode. The equivalent circuit for mode II is shown in Figure.6.6 (b).

6.5.2. $i_L^* < 0$, Switch S_4 is always ON

Mode III ($-i_l > -i_L^* + h$): (S_3 & S_4 ON)

In mode III, the inductor L gets charged in the negative direction. RES will supply the current and the path will be through S_3 , S_4 and the grid. Current injected to grid will be negative in this mode. The capacitor C_f gets charged in the negative direction. Current will increase till it reaches the lower hysteresis limit. Figure.6.6(c) depicts the circuit diagram corresponding to mode III.

Mode IV ($-i_l < -i_L^* - h$): (S_3 OFF & S_4 ON)

Figure.6.6 (d) shows the equivalent circuit for this mode. Here, since the inductor current reached the lower hysteresis limit, the switch S_3 gets turned OFF. S_4 remains in the ON condition. Stored energy in the inductor gets discharged throughS_4 , body diode of S_2 and the grid.

Here it can be seen that only one switch is operating at high frequency at a time. The switching stress and switching loss will be very less for this reason. Current control operation will ensure a distortion less injected current since the injected current itself is the control variable here. Inductor charges positively in mode I and discharges in mode II. Similarly, in Mode III the inductor charges negatively and discharges in the mode IV. The grid connected operation of inverter is achieved with the current control method explained. In the off grid or islanding mode of operation of the inverter, similar current control method can be implemented with a modification in reference current generation.

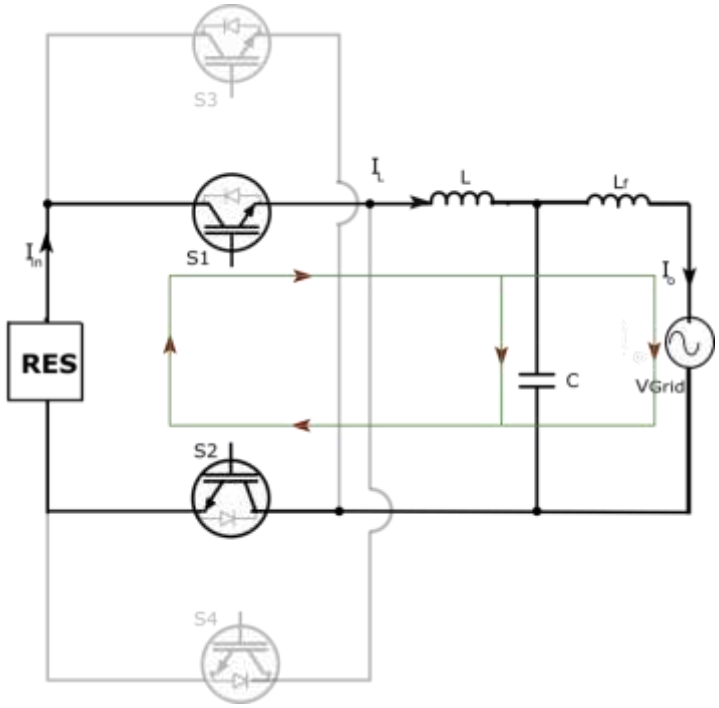

Figure 6.6(a) Mode I operation of proposed grid tied FSILI

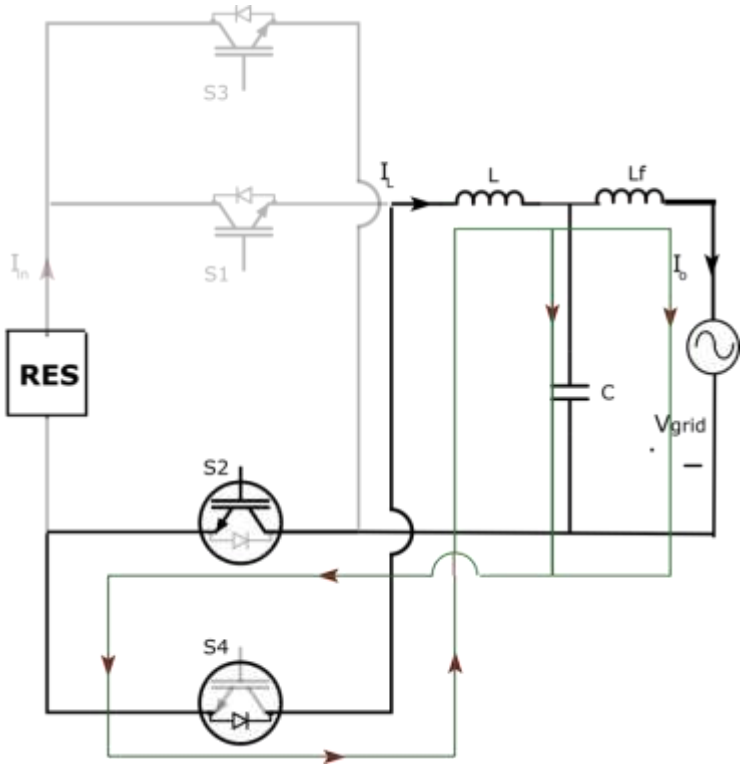

Figure.6.6. (b) Mode II operation of proposed grid tied FSILI

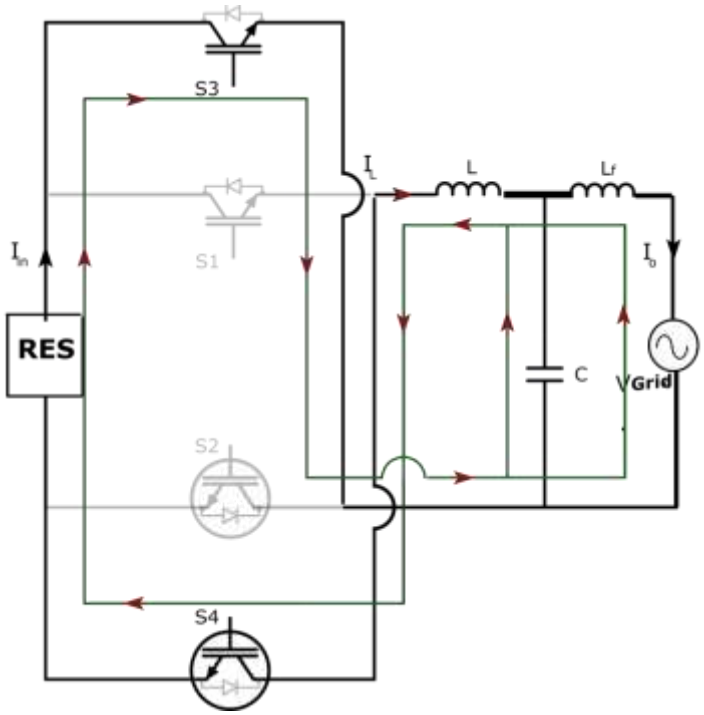

Figure6.6(c).Mode III operation of proposed grid tied FSILI

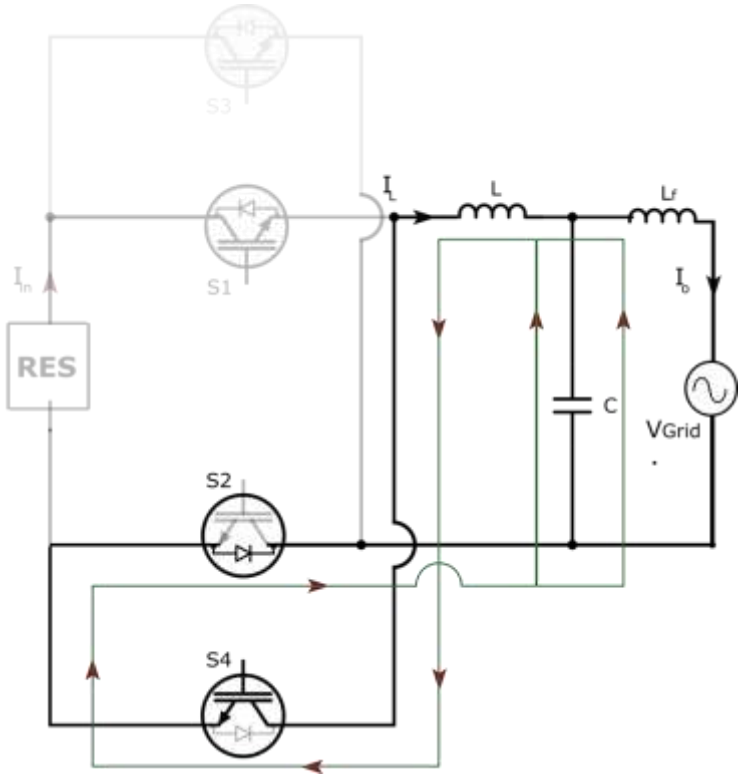

Figure 6.6(d) Mode IV operation of proposed grid tied FSILI

6.6. Islanding Mode Operation of the Proposed FSILI

In the islanding mode operation of the proposed inverter, the capacitor voltage V_{cf} is sensed and is compared with$V_{cf}{}^{*}$ .Error being fed to PI controller to generate the $i_L{}^{*}$. Remaining control implementation is same as explained in the proposed grid control method.

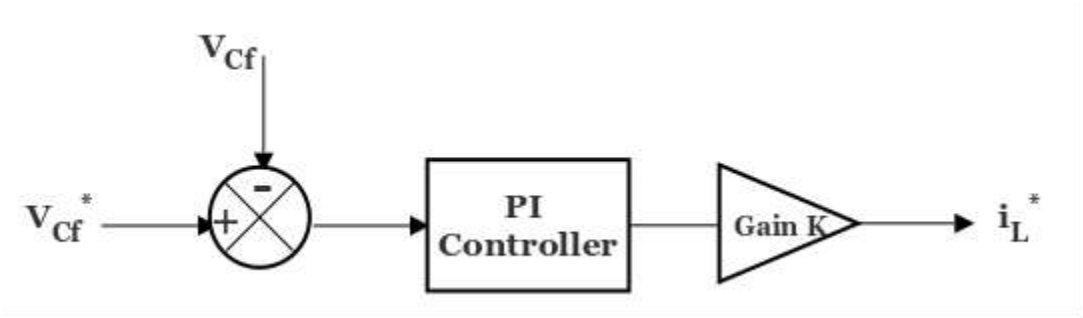

Figure.6.7 Block diagram of $i_L{}^{*}$ generation from the capacitor voltage.

6.7. Simulation of Proposed FSILI in Grid Connected and Islanding Mode.

In this section the simulation of the proposed FSILI in the islanding mode and grid tied mode is explained. Simulation of current control and proposed grid control techniques are explained with the inferences. Input voltage of the RES is chosen to be 325V DC. A single phase grid with parameters 230V, 50Hz is considered here. Simulation parameters are given in Table 6.1. In the first section, the simulation with stand-alone mode is explained.

Table.6.1. Simulation Parameters of FSILI in grid connected and islanding mode.

Parameters	***Values***
Input Voltage V_{dc}	325V
Inductor, L	20mH
Inductor, L_f	20mH
Capacitor, C_f	0.6μF
Load Resistance, R(for islanding mode)	100Ω

6.7.1. Simulation of Islanding Mode Operation of the Proposed FSILI

Proposed FSILI is operated in the islanding mode with the current control technique described. The capacitor voltage reference is varied from $160V_{rms}$ to $230V_{rms}$. at 0.7 sec. The PI controller will tune to respond for the transient in the reference voltage and the current reference i_L^* is generated. Figure.6.8. shows the output voltage response for transient change in the reference voltage. The exact tracking with minimum settling time is obtained. Figure.6.9 shows the output current response. The zoomed view of the output voltage is shown in Figure.6.10. Output voltage tracks the variation in the reference RMS value of capacitor voltage and settle down to the new reference value. Instantaneous output shown in the zoomed view indicate the tracking clearly.

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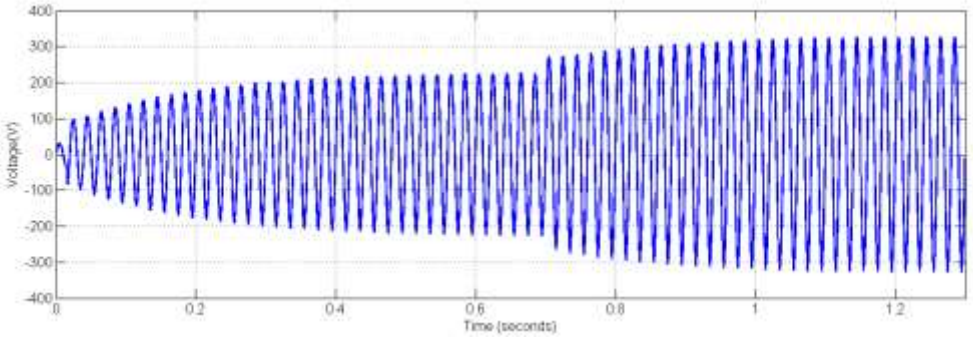

Figure.6.8.Output voltage response with a transient change in reference voltage at 07.sec

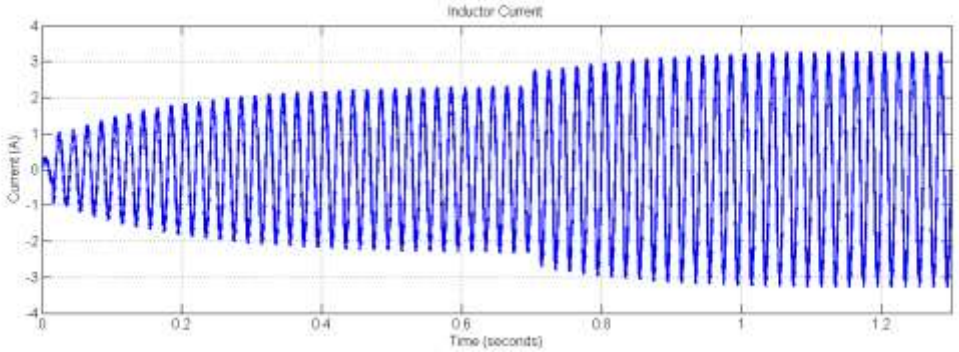

Figure.6.9.Inductor current response with a transient change in reference voltage at 07.sec

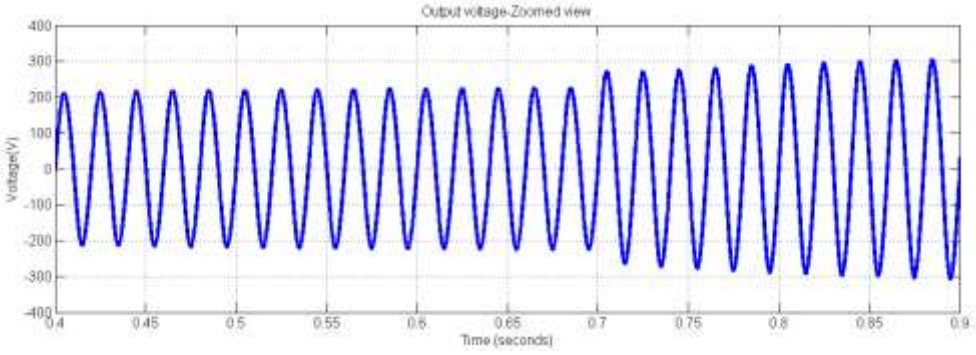

Figure.6.10.Zoomed view of output voltage with transient change at 0.7 sec

The FFT analysis of the output voltage and current indicate the quality of the output obtained. Figure.6.11.shows the THD obtained, and the value is 2.15% which is within the IEEE limits.

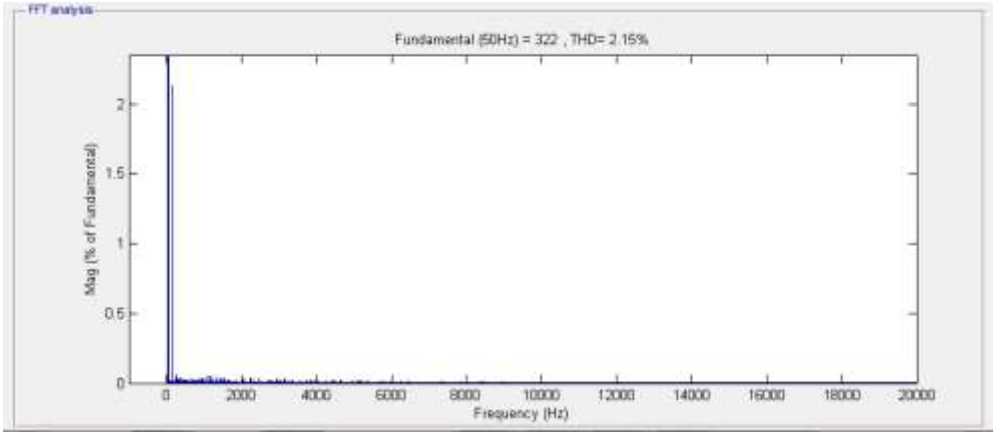

Figure.6.11.Frequeny spectrum of output voltage for current controlled FSILI.

6.7.2. Simulation of Grid Connected Operation of FSILI

In this section the simulation of the proposed four switch infinite level inverter under grid connected mode is discussed. Simulation parameters are given in Table.6.1. Reactive power delivered / absorbed is taken to be zero to ensure the unity power factor operation while injecting power. Simulation is carried out for two different injected power levels. When an active power of 530W is injected on to grid, the rms value of injected current is obtained to be 2.3 A. The peak current is 3.25A.Figure.6.12.shows the injected current, grid voltage and injected power. The injected current, inductor current and capacitor current waveforms are shown in Figure.6.13.The FFT analysis of the injected current is carried out to understand the quality of the injected current. The THD is obtained to be 3.94 % which is well within the IEEE standards which is shown in Figure.6.14.

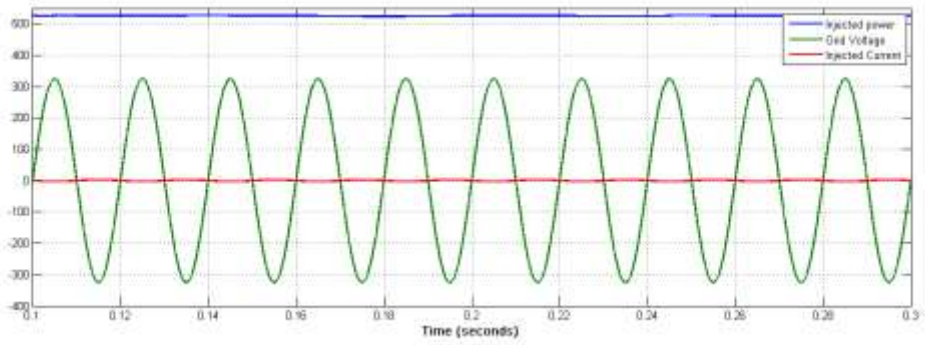

Figure 6.12.Injected power, Injected current and Grid voltage waveforms for an active power injection of 530W

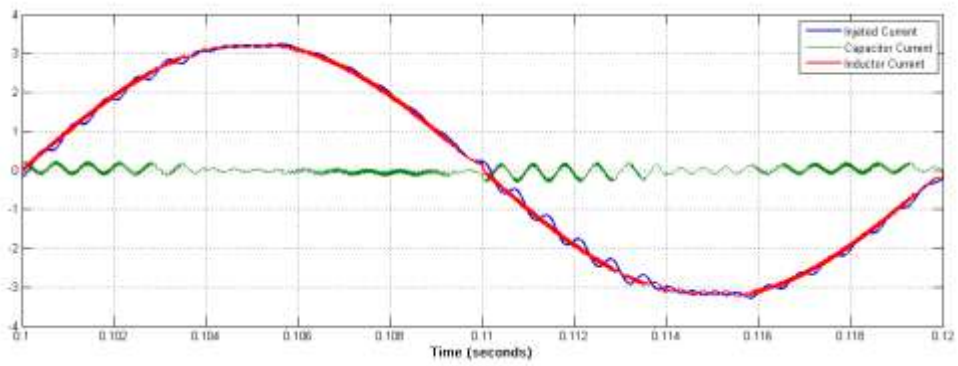

Figure.6.13. Injected current, Inductor current and Capacitor current waveforms for an active power injection of 530W

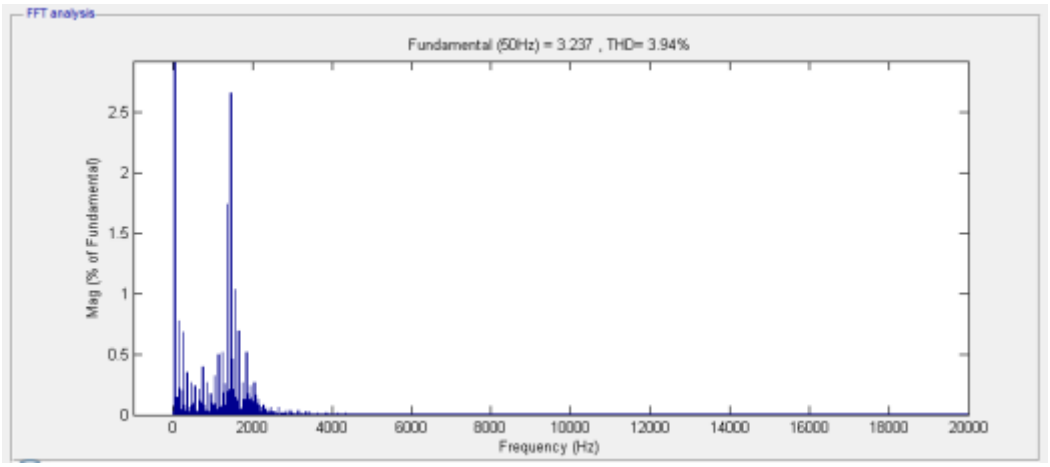

Figure.6.14. FFT analysis of injected current for an active power injection of 530W

To further understand the power injection capability, simulation is carried out for an injected power of 265W. Figure.6.15. show the injected power, injected current and grid voltage wave form for a power level of 265W. Inductor current, injected current and capacitor current waveforms are given in Figure.6.16. The FFT analysis is done for the given power level and THD is obtained to be 2.65 % which is shown in Figure.6.17.

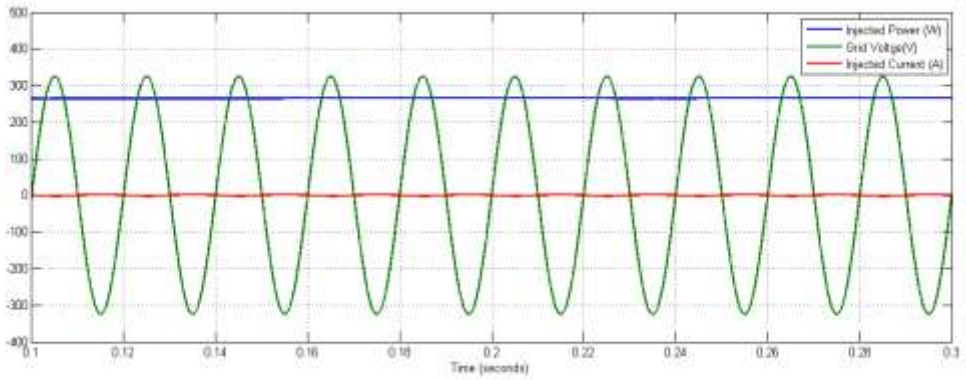

Figure.6.15. Injected power, Injected current and Grid voltage waveforms for an active power injection of 265W

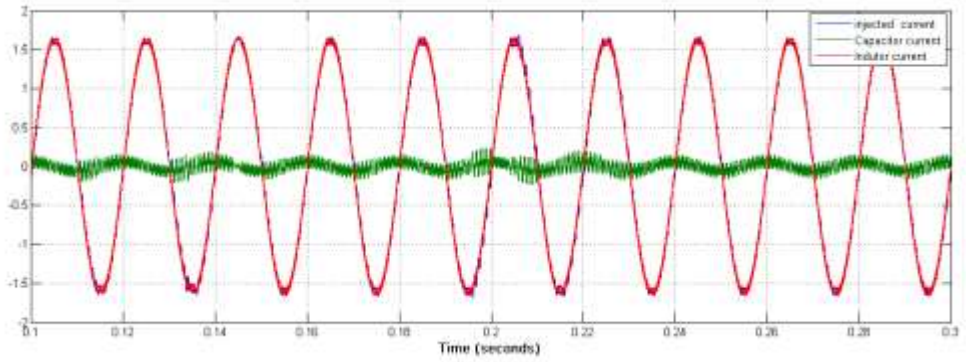

Figure.6.16. Injected current, Inductor current and Capacitor current waveforms for an active power injection of 265W

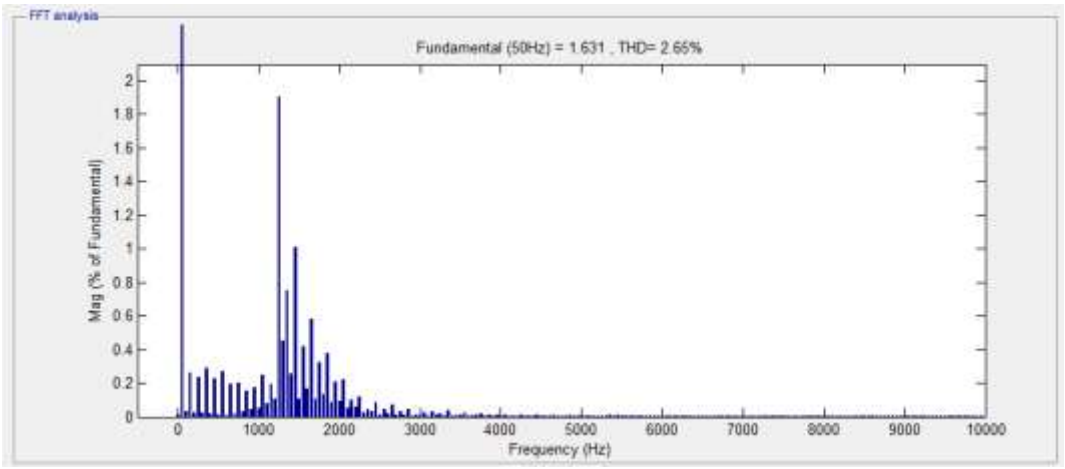

Figure.6.17. FFT analysis of injected current for an active power injection of 265W

When the grid is loaded with a resistive load of 10ohm, the load current will be 32A (peak).The inverter injected 2.3A (rms) current on to the grid and the remaining power is taken from the grid. The injected current, grid current and the load current is shown in Figure.6.18.The inverter voltage is found to be exactly in phase with the grid voltage.

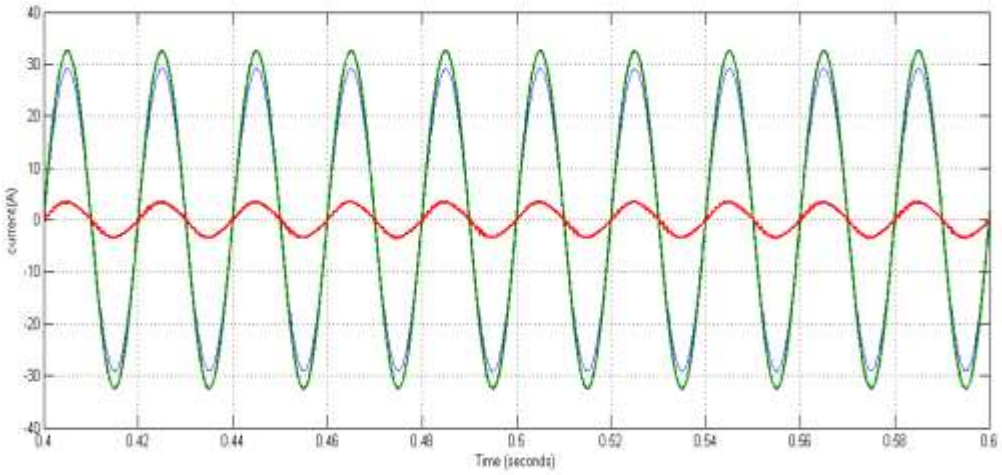

Figure.6.18. Injected current, Grid current and Load current-R load

Power injected to grid can be controlled with the proposed grid control method. For the case considered here for simulation, power injected to the grid is 530W and 265W. With the available rating of the inverter and the supply, the injected power can be varied. .

To further investigate the quality of injected current a comparative analysis with IEEE 519 and IEEE1547 standard is done. As per IEEE 519 and 1547 standards, the limit of harmonic components allowable in the inverter output is decided based on the ratio of short circuit current of inverter to the full load current. For $I_{sc}/I_L < 20$, the allowable Total Demand distortion (TDD) or Total rated current distortion (TRD) is to be less than 5%. Individual harmonic components are also specified to be within the limit given. TRD or TDD is different from THD but for the analytical simplicity, since I_{rated} is almost equal to I_1 in the given case it is assumed to be equal to THD. Figure 6.19 shows the harmonic components with their percentage of injected current for a injected power of 530W.

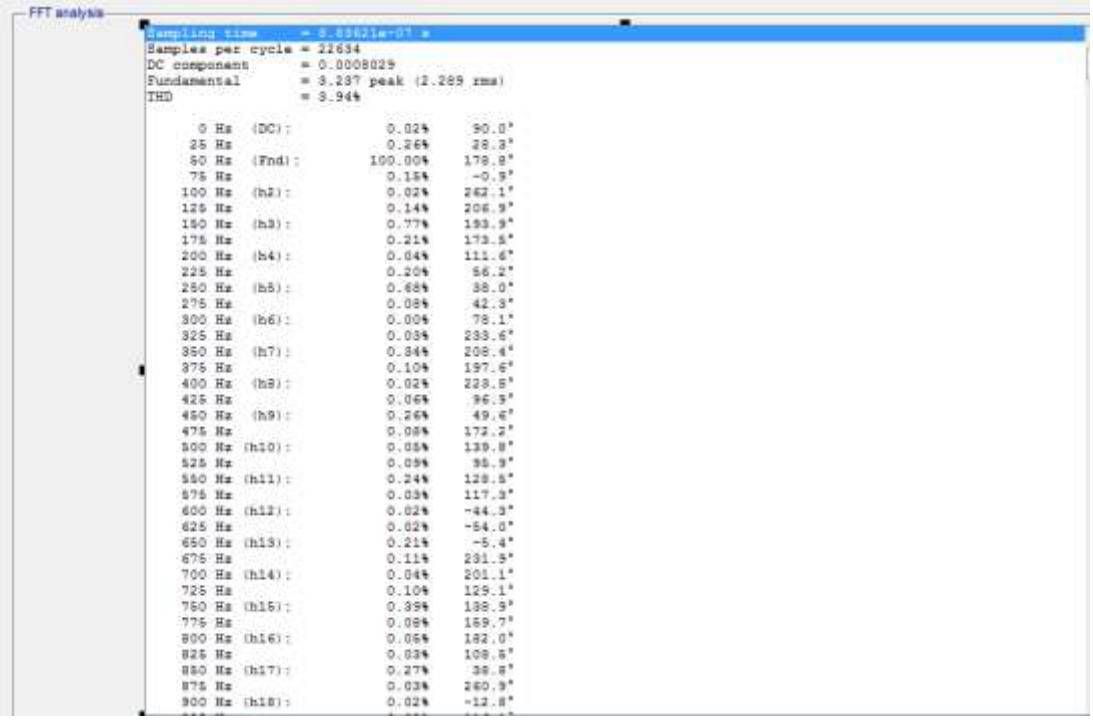

Figure.6.19. List of percentage harmonic components in the injected current for 530W

There is rule of thumb for finding short circuit current of inverter according to Kroposki (2008), Dugan et al. (2002), that it will be one to two times the full load current for one cycle or less. The full load current of inverter is approximately 2.3A (rms) and the corresponding power injected is 530W. The short circuit current is obtained to be approximately 4.6A. For the two cases of power injection explained(530W and 265W) the ratio of short circuit current to load current is obtained to be approximately 2 and 4 which is less than 20. So, the TRD/THD should be less than 5%.Table 6.2.gives comparison of the percentage of harmonic components present in the injected current with the standard values.

Table 6.2. Comparison of harmonic components in injected current with standard values

	h<11	**11≤ h <17**	**17≤ h ≤ 23**	**THD**
% of harmonic component in injected current as per IEEE 519 Standard	4.0	2.0	1.5	5
% of harmonic component in injected current (530W)	3.3	1.32	1.69	3.94
% of harmonic component in injected current (265W)	1.17	0.59	0.45	2.65

Table clearly shows that the harmonic components in the low frequency range are well within the standards. Also, the THD obtained in two cases are less than 5%. In case of 530W injection there is a slight variation with the standard value which needs to be addressed in the practical implementation.

6.8. Summary

In this chapter the grid tied operation of the proposed Four Switch ILI is described. To extract power from renewable sources, the grid control operation is to be carried out. Here a hysteresis current control method is implemented with real and reactive power flow control. The analysis of the proposed grid control method is discussed in detail. The simulation is carried out and the results are given which validates the effective injection of power to grid. From the simulation study it is clear that the proposed grid tied infinite level inverter topology is a viable solution for the integration of extracted power from RES to grid. The harmonics are well within the standards and also, the implementation is very simple with hysteresis current controller used. It is advantageous that the proposed FSILI can be operated in the islanding mode also with the current control technique. The power that should be injected to grid can be controlled using the proposed grid control technique. In the next chapter hardware implementation of the proposed FSILI is discussed.

Chapter 7

Hardware Implementation of Proposed FSILI

7.1. Introduction

To verify the theoretical analysis and simulation study, a hardware prototype is developed for the proposed FSILI. For prototype building and testing National Instrument's data acquisition cards (DAQ) are extensively used in laboratories because of their accurate performance. For the control implementation of power electronic systems, NI's DAQ can be better solution. Capability of high end parallel processing, reconfigurable hardware, high computational speed and low cost are some of the reasons for the extensive use of National Instrument's DAQ cards. Here, the hardware implementation of proposed FSILI is carried out using PCIe6363 DAQ card which is incorporated along with the Simulink Desktop Real time tool box of Matlab/Simulink. The connector used here is NI SCB 68A connector. The digital pulses to the switches are given TLP250 driver circuit through the connector. Hardware implementation of the proposed FSILI is discussed in this chapter.

In section 7.2.various components used for the hardware implementation are explained. In the subsequent section (section 7.3.), design of hardware components are given. In section 7.4., experimental setup for the hardware implementation is explained. Experimental results obtained are given in section 7.5. Concluding remarks of the chapter are given in section 7.6.

7.2. Components used for Experimental Validation

For the experimental validation of the proposed FSILI topology, the experimental setup is built with different components. Control implementation is done with NI's PCIe6363 card. Input DC supply is given with the help of a rectifier module. The inductor is wound for the particular value as per the design. Capacitor is selected

as per the design and a resistive load is applied to the inverter. Details of different components used in the experimental setup are given in this section.

7.2.1. Semikron IGBT Power Stack

Semikron IGBT power stack is used to rectify the available AC supply and to feed the FSILI with required voltage. An autotransformer at the AC input side will regulate the input voltage of the rectifier. The rectifier module maximum output voltage is 600V DC. Figure.7.1. shows the Semikron IGBT module used in the setup.

Figure.7.1. Semikron IGBT Power stack.

7.2.2. FGA25N120ANTD – IGBT Switch

Proposed FSILI consist of four IGBT switches. Switches should have antiparallel diodes and should be capable of handling high voltage and current. The switch chosen here is FGA25N120ANTD, which is having a voltage rating of 1200V and current rating of 25A. The diode is also capable of carrying high current in the forward biased condition (25A at 100^0 C). Also, the reverse recovery time of the IGBT selected here is small. So, there will not be any reverse recovery issue associated with the body diode. Figure.7.2. shows the selected IGBT.

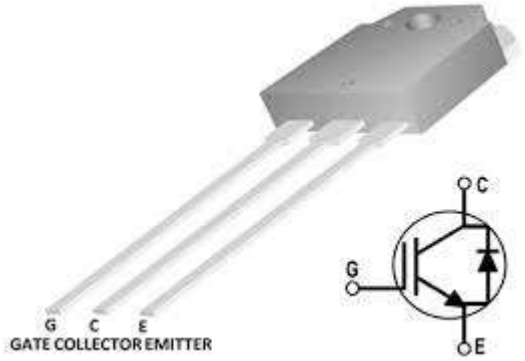

Figure 7.2.FGA25N120ANTD IGBT switch

7.2.3. Gate Driver Circuit.

For the proposed FSILI, there are 4 IGBT switches, each requires separate driver circuit. These TLP250 drivers should be supplied with isolated DC input of 15V. Power supply unit with LM7815 IC will be used. Multi turn transformer is used before the rectifier stage of power supply to obtain isolated DC for the drivers. Figure 7.3.represents the pin out diagram of TLP250 driver circuit.

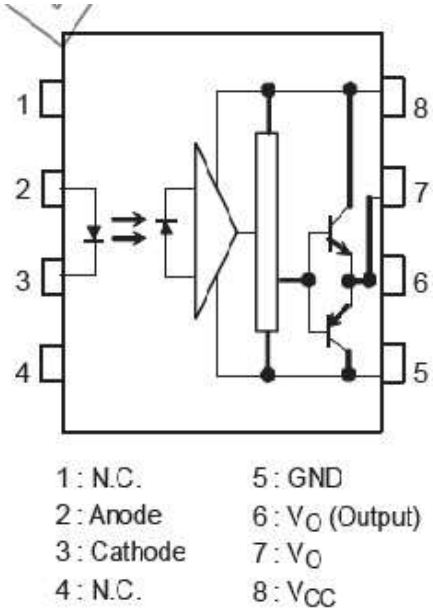

Figure.7.3. Pin out diagram of TLP250

7.2.4. DAQ – PCIe 6363 with Custom Cable

PCIe 6363 is the interface used to communicate with the Simulink Desktop Real time tool box of Matlab/Simulink. On the basis of real time signals received, the switching pulses will be generated by real time tool box of Matlab. In open loop, the pulses will be generated internally. Figure.7.4. shows the DAQ card PCIe 6363.

Figure.7.4.PCIe6363 DAQ card

The DAQ will be given to a connector which will be having analog and digital terminals by which the Real time toolbox of Matlab can communicate with peripheral circuits. Here, SCB- 68A connector is used.

7.2.5. 68-Pin Shielded Connector Block:

The SCB-68A, shown in Figure 7.5, is a shielded I/O connector block with 68 screw terminals for easy signal connection to a National Instruments 68-pin or 100-pin DAQ device.

Figure 7.5.NI SCB-68A connector

7.3. Hardware Design

In the hardware design, the number of turns of inductor is found out. Also, the capacitance value is obtained from the corresponding equation. Switch selection and other details were discussed in previous section.

Inductor Design

From the flux equation of inductor,

$$E = N\frac{d\phi}{dt} = NA_e\frac{\Delta B}{\Delta t} \tag{7.1}$$

Where N is the number of turns, ϕ is the flux

Also, from EMF equation,

$$E = L\frac{di}{dt} \tag{7.2}$$

Therefore by combining two equations, $N = \frac{L}{A_e}\frac{\Delta I}{\Delta B}$ (7.3)

Where $\Delta B = 0.3T\ to\ 0.6T$ (For limiting saturation)

ΔI is the peak to peak inductor current ripple

Ferrite core E55 is selected. So, core cross sectional area, $A_e = 420mm^2$

$\Delta B = 0.3$, The inductance value is obtained to be 20mH for an inductor current ripple of 0.4A. (From equation 4.16)

By substituting the values in equation 7.3 number of turns is obtained as N=63

The air gap length, l_g can found out from the equation, $L = \frac{N^2}{\frac{l_g}{\mu_0 A_e}}$

From that $l_g = \frac{N^2}{\frac{L}{\mu_0 A_e}}$ (7.4)

By substituting the values of number of turns, inductance, permeability of free space and cross sectional area of core, air gap length in the magnetic circuit can be found.

$$l_g = 0.104mm$$

Selection of Capacitor

Capacitor value is selected on the basis of equation 4.17.and it is obtained to be 0.6μF.

7.4. Experimental Setup of Proposed FSILI

Figure.7.6. shows the hardware control block of proposed inverter. Hardware specification is given in Table 7.1. IGBT switches with antiparallel diode are used as power switches. Inductor is designed with ferrite core to get 0.02H with 63 turns. Capacitance value is chosen as 0.6μF. Control pulses for the inverter are generated by Simulink Desktop Real time tool box of Matlab/Simulink. Real time pulses are fed to the inverter switches through the interface card PCIe 6363. From the connector SCB-68A, the digital pulses are given to the TLP250 driver circuit. The driver will provide required isolation between power circuit and control circuit

Table 7.1.Hardware .Specifications

Parameters	***Specifications***	***Values***
Rectifier Module (Input Supply)	Semikron IGBT power stack(600V DC) for rectification	325V
Inverter Switches	IGBT FGA25N120ANTD (25A,1200V)	
MOSFET Driver	TLP 250	
Controller	PCIe6363 with Real Time windows Target	
Inductor	Ferrite Core(E55)	20mH
Capacitor	AC capacitor	0.6μF
Load Rheostat		100Ω, 5A

Experimental setup for the proposed FSILI is given in Figure 7.7. A three phase autotransformer is used to provide the AC supply for the rectifier module. The semikron IGBT power stack is used as rectifier module here. It can obtain DC voltage upto 600V. Autotransformer is adjusted to obtain input DC voltage (325 V) for the inverter

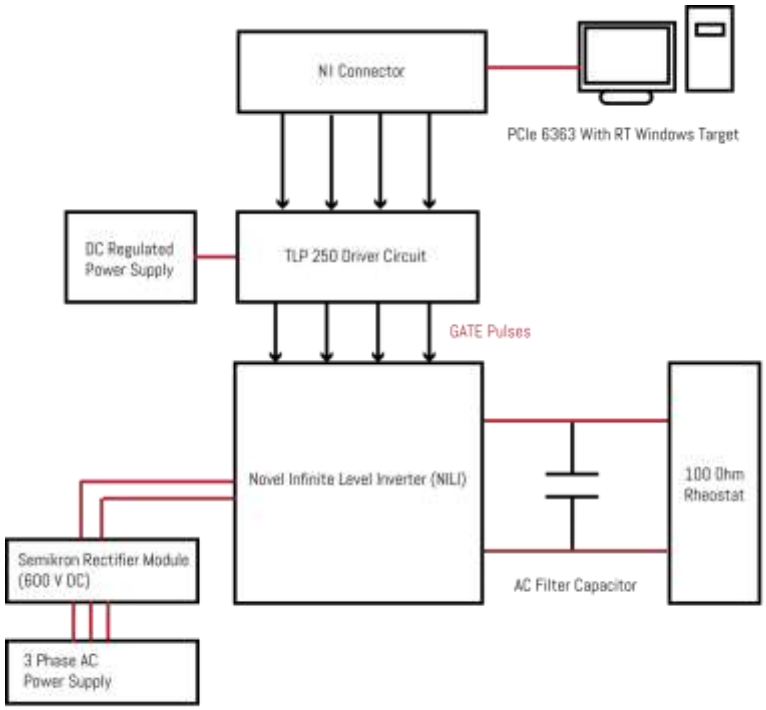

Figure 7.6.Hardware control block of proposed FSILI

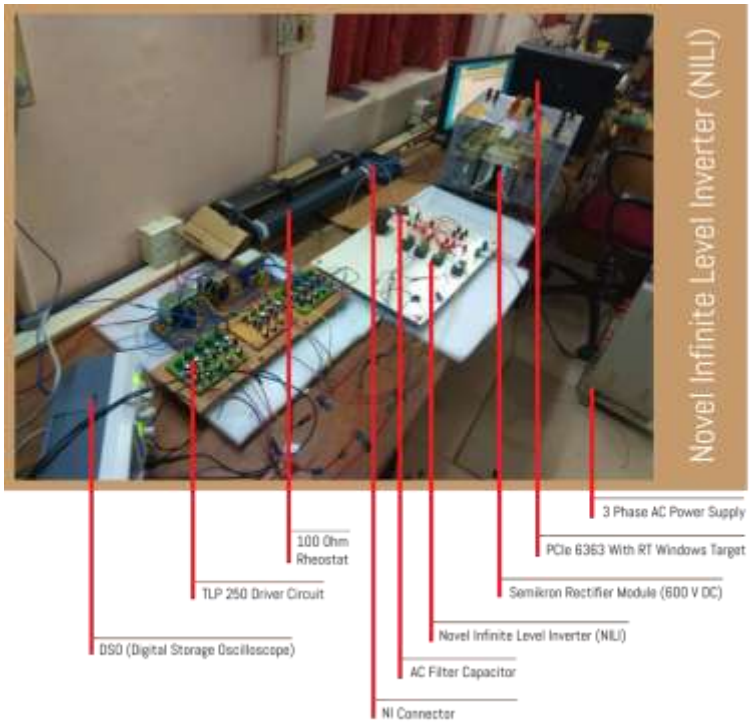

Figure.7.7. Hardware Setup of proposed Novel Four switch Infinite Level Inverter

7.5. Experimental Results

To ensure the practical feasibility of the proposed FSILI experimental study is carried out with the given specifications. A resistive load is used here in the setup. Control pulses are generated and were applied through the gate driver circuit.

Figure 7.8.represents the switching pulses applied to the proposed FSILI. Two among the four gate pulses are high frequency signals. Other two operate at fundamental frequency reducing the switching loss. Figure 7.9.shows the output voltage wave from. RMS output voltage is obtained to be 232V. Figure7.10. depicts the output current waveform. RMS value of output current is obtained to be 2.34A for the given 100 ohm resistive load. The inductor current is displayed in Figure 7.11. Zoomed view of inductor current is shown in Figure.7.12. From figure it is clear that the inductor current is continuous. It can also be understood that the ripple content in inductor current will be maximum at $\pi/6$ angle. Input current waveform is shown in Figure 7.13. Input current is discontinuous whereas the inductor current is continuous.

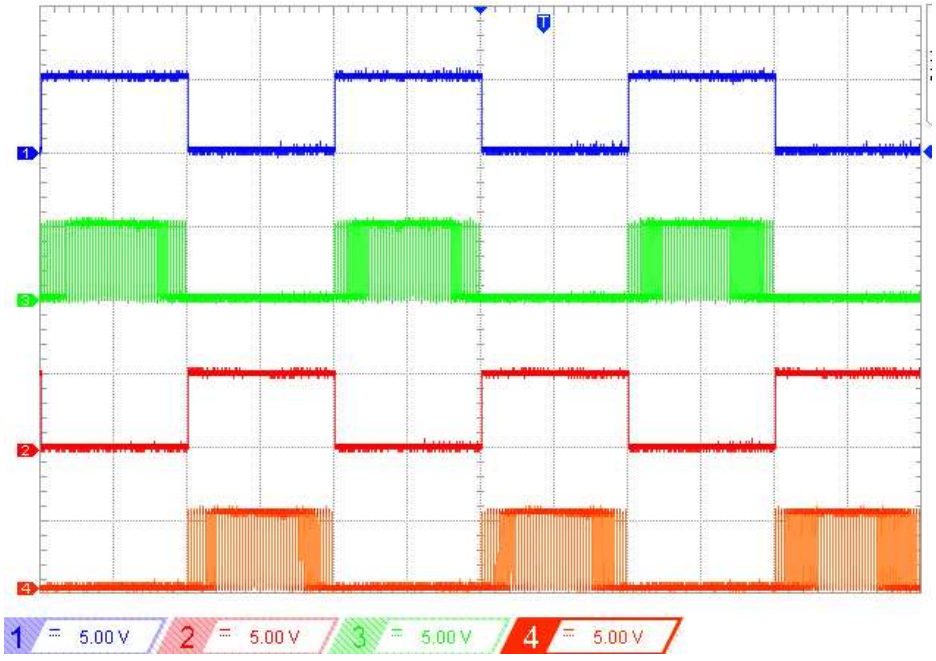

Figure.7.8. Switching pulse waveforms

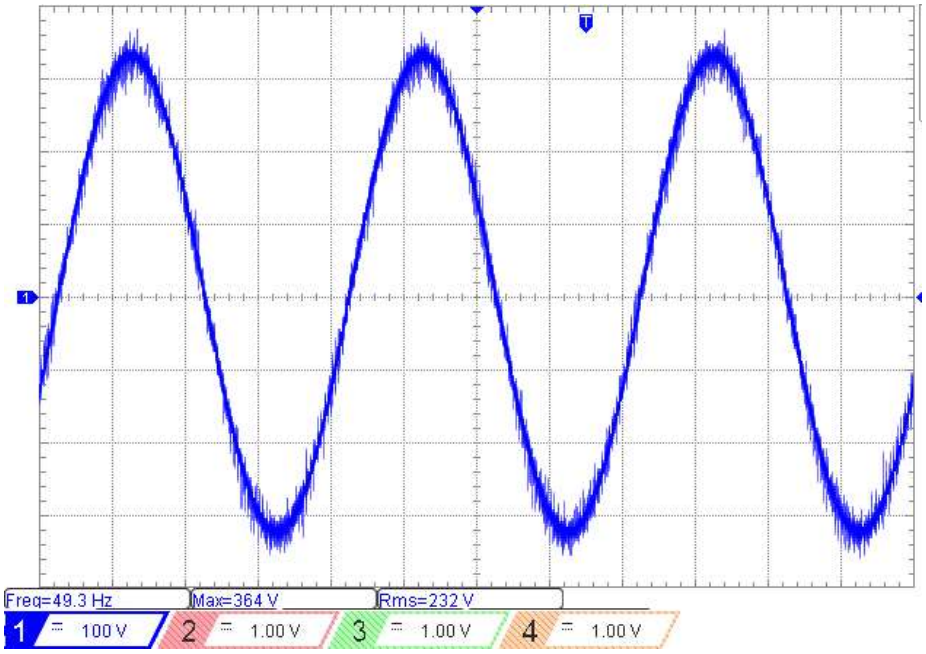

Figure.7.9. Output voltage waveform of FSILI

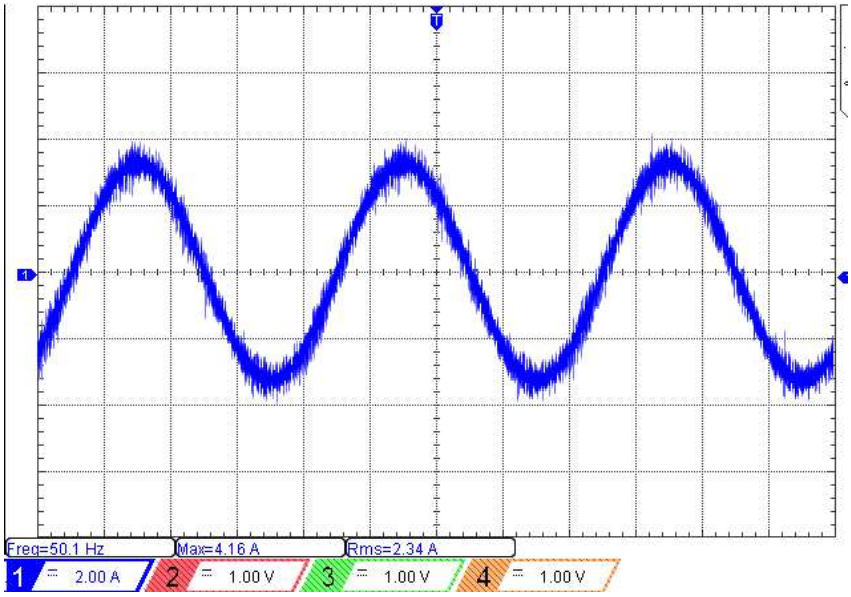

Figure.7.10.Output current waveform of FSILI

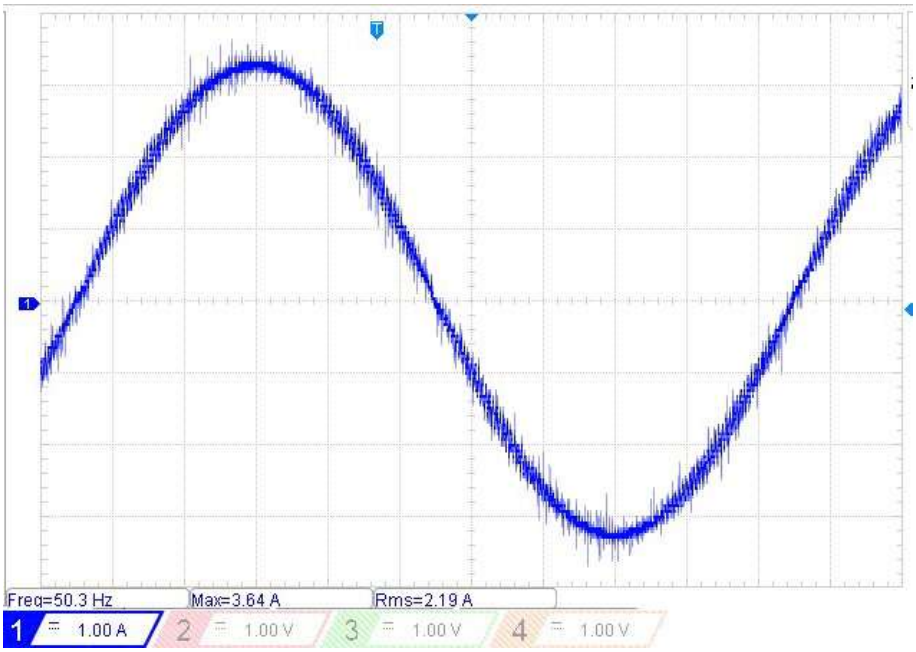

Figure.7.11. Inductor current waveform of FSILI

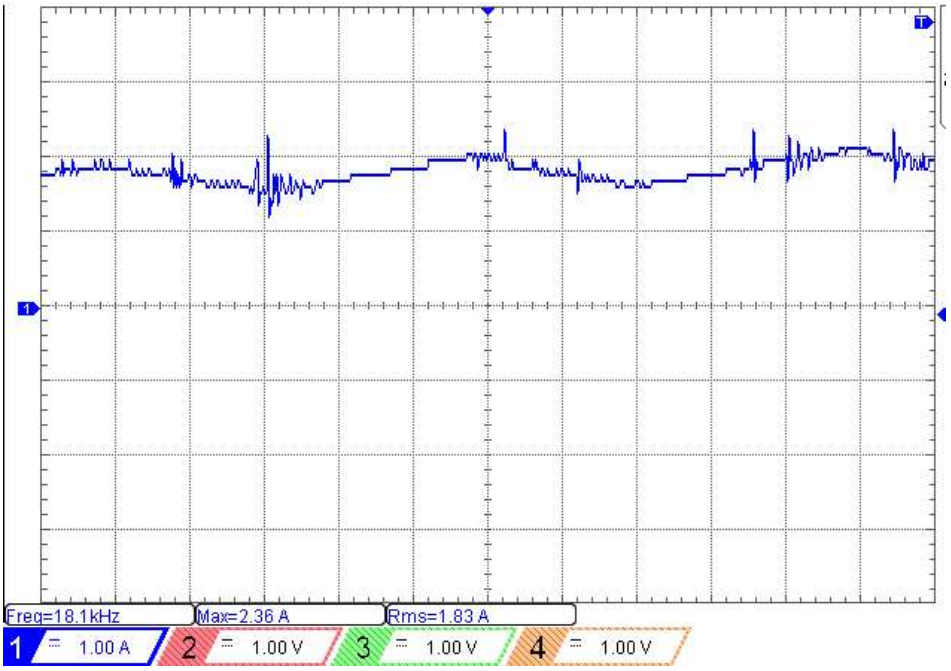

Figure.7.12.Zoomed view of inductor current

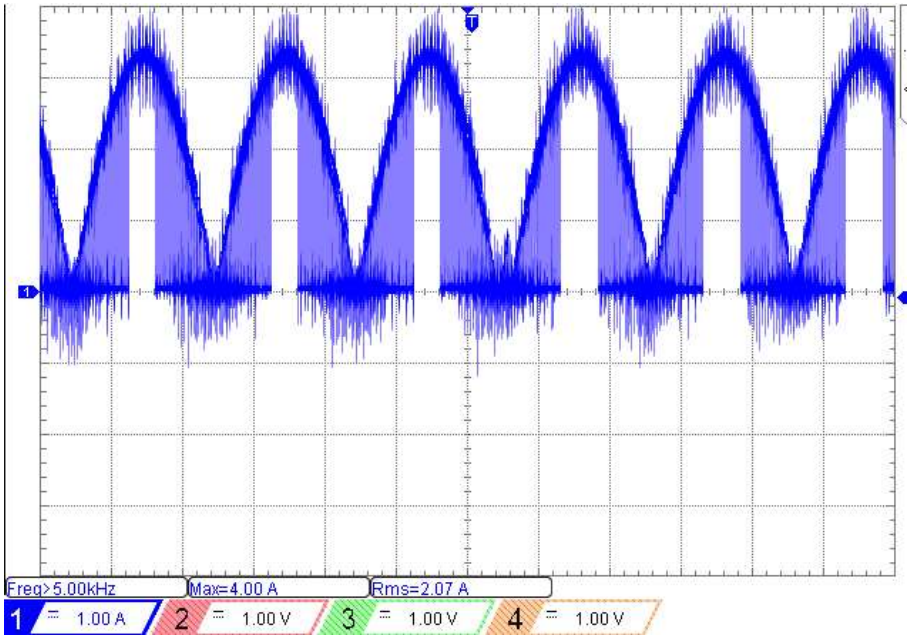

Figure7.13. Input current waveform of FSILI

From the results obtained it is clear that high quality AC is obtained in the output using the proposed inverter. The results are exactly in complement with the simulation result obtained. The inductor current and input current also matches with the simulation result.

7.6. Summary

Experimental setup and hardware results of proposed FSILI are discussed in this chapter. Hardware implementation of proposed FSILI is carried out using PCIe6363 DAQ card implemented along with Simulink Desktop Real time tool box of Matlab/Simulink. Control pulses are obtained with the real time windows target and are applied to the inverter through NI SCB-68A connector and the gate driver. Pulses are obtained to be in accordance with the theoretical derivations. Inverter output voltage is obtained and is found to be same as obtained in simulation study. Near sinusoidal output voltage and current is obtained using the proposed FSILI. Inductor current shows the charging and discharging of buck circuits. Inductor current is continuous and the input current is discontinuous in nature. Proposed inverter is having fewer harmonic and is a good candidate for critical applications. Grid tied operation and drive implementation of the proposed inverter can be done.

Chapter 8

Conclusions and Future Works

8.1. Introduction

A novel inverter topology capable of producing distortion free AC with minimum components and switching loss is designed, its control developed and implemented. The inverter is said to have infinite levels depending upon the carrier frequency, hence the name Infinite Level Inverter (ILI). As the topology is a modification of conventional ILI with reduction in switches and improvement in the output quality, the proposed topology is termed as Novel Four switch Infinite Level Inverter (FSILI). A three phase inverter topology is also derived from the proposed novel FSILI. Novel three phase ILI topology has least DC bus requirement in comparison with different control methods of VSI. For applications having limitations in DC bus availability, the proposed three phase topology is a viable solution. Also, the grid tied operation of the proposed FSILI with a simple and effective grid control method is proposed. Hardware prototype of the proposed FSILI is implemented using National Instruments PCIe card.

Constant demand for quality AC invited the researchers to contribute more on the development of inverter topologies. Most of the electrical load available now works in AC supply. Also, the increased use of energy may drain out the available nonrenewable sources in the near future. The current scenario of the renewable energy sources was reviewed. It is found that there is a drastic increase in the use of renewable sources all over the world and in particular in India. Methods for the extraction of available renewable sources also reviewed and it is seen that extraction to the form of electrical energy is the most effective method since electrical energy can be converted into any form and can be transported to any distance with ease. The grid systems are mostly AC in nature and thus the extracted power, from any source like solar, wind, fuel cell etc should be converted into AC for which inverters are essential. Different power extraction schemes were reviewed and there are different topologies of inverters available for power extraction and for utility applications. Inverter topologies were analyzed on the basis of the number of switches, nature of output obtained, control complexity etc. Basic

topologies suffer from high harmonic distortion, need for heavy filtering, presence of additional impedance network etc. From the analysis, it was found that multilevel inverters were emerged as a solution for the harmonic problems, switching stress and EMI issues etc. The basic MLI topologies were reviewed and it was observed that while improving the output quality, either number of components (switches, diodes or capacitors) or number of sources was increased when the output approaches sinusoidal form. Different modulation techniques employed in MLIs were also reviewed. Some other multilevel inverter topologies available in the literature were also studied which focus mainly on reduction of circuit complexity while providing good quality output. Control methods for the grid integration of inverters were also reviewed. PI, PR, SMC and Hysteresis control were seen in the literature for the grid control of inverters. Different algorithms for the control of injected power were also reviewed. Synchronization with and without PLL were also observed in the literature.

8.2. Summary and Major Findings

Review of existing topologies and different control methods has led to the scope of introducing a new simple and improved inverter topology for the utility applications and grid integration. Infinite level topologies were further modified with the introduction of the proposed topology with a further reduction in the harmonics and switching loss. Three phase four switch infinite level inverter has the advantage of improved DC bus utilization is suitable for drive applications. Grid control method for the proposed topology utilizes the hysteresis current control and a simple power control algorithm. Reduced number of switches, simple and effective control high DC bus utilization, and reduced harmonic content are some of the key takeaways of the proposed Novel Four Switch ILI topology.

8.2.1. Conventional Infinite Level Inverter Topology

Analysis of the conventional infinite level inverter topology was carried out for both single phase and three phase circuits. Only one switch per phase was found to operate at high frequency thus the switching loss was minimal compared to MLI and traditional VSI. The three phase ILI topology additionally had high DC bus utilization.

400V RMS in the line voltage was obtained with a DC link voltage of 325V. FFT analysis was carried out for ILI with R load and RL load and the THD is found to be less than 2% both for voltage and current under all load conditions. Thus, the topology was observed to be suitable for applications like electric drives, grid control and compensation, UPS applications etc. It was found to have redundancy in the switch count for the conventional ILI and with some modifications, one switch and one diode can be eliminated thus a reduction in the size; cost and loss can be achieved. Unfolding using H bridge inverter caused to have ripple at the zero crossing instances and the harmonics increased because of this. The topology was found to be an alternative solution for MLIs and traditional inverters but observed to have some demerits also.

8.2.2. Novel Four Switch Infinite Level Inverter

From the analysis carried out on the conventional ILI topology it was found that there were some limitations which can be rectified with certain circuit modifications and by applying a modified PWM. Thus with some modifications in ILI, a Novel Four Switch Infinite Level Inverter (FSILI) was introduced and whose design and analysis were carried out. The topology was found to have only four switches and there is no additional diode required for the operation. With the modified PWM technique only one switch was found to operate at high frequency so the switching loss is same as the conventional ILI. Unfolding issue with conventional ILI was eliminated here and two separate buck circuits were operational at a time. For the similar parameters as for the conventional ILI, FFT analysis was carried out and it was found that the THD was near to 0.5%, and it is found to be very low in comparison with conventional ILI. So analytically it was found that the proposed FSILI is having all the good of conventional ILI and also was able to eliminate most of the drawbacks. Hardware implementation of the proposed FSILI was also carrier out with National Instrument's PCIe control card. Experimental validation of the theoretical and simulation study was under taken and the results are found to be exactly in line. The experimental study was done with real time tool box of Matlab/ Simulink with PCIe card and connector. TLP driver circuit was also used to provide necessary isolation. The results were promising and practical models are to be developed to address the real time scenario.

8.2.3. Novel Three Phase Infinite Level Inverter Topology

A three phase derivation of the novel FSILI was investigated and it was found to have equal DC bus utilization as that of conventional three phase ILI. The novel three phase FSILI was modulated with third harmonic injection PWM to increase the DC bus utilization further and was found to have a 400V rms line voltage with 282V in the DC link. The drive performance was also investigated and with double ended induction motor and was found to be satisfactory. The FFT analysis was also carried out with R and RL load and it was found that the THD was in the range of 0.5% and was very low compared with conventional three phase ILI. One switch per phase got reduced here in comparison with the conventional ILI.

8.2.4. Grid Tied Operation of Novel Four Switch Infinite Level Inverter

Novel four switch infinite level inverter was found to have low distortion in the output and is a promising candidate for the renewable power extraction. A grid control algorithm for the FSILI was proposed. The current control was simple and was done with a hysteresis controller. A unity power factor active power injection algorithm without complicated PLL structure was proposed. Islanding mode of proposed FSILI with current control was derived. Analytical study was verified with simulation for both islanding and grid connected mode and it was found that the inverter with the proposed control was able to inject power at unity power factor. Different power levels were chosen for the injection and were found satisfactory. So proposed FSILI was found to be a good candidate for injection of power onto grid extracted from renewable sources and was capable of active power control at unity power factor.

8.3. Major Research Contributions

The research work analyzed the infinite level inverter topology on the basis of output quality and switch count. To overcome the shortcomings of the conventional topology a novel four switch inverter topology was proposed.

The major research contributions can be enumerated as below

- A novel Four Switch Infinite Level Inverter (FSILI) was proposed and design and analysis carried out. Reduction in switch count and low harmonic distortion are the key features of the proposed topology. Comparison with conventional ILI shows the improvement in THD with reduction in switch count.
- Closed loop control and various regulation analyses ensured the robustness of the inverter with disturbances.
- A Three Phase Infinite Level Inverter was derived from the proposed Four Switch Infinite Level Inverter which is having high DC bus utilization same as the conventional ILI with reduced switch count and improved harmonic elimination. Switching losses were same as conventional ILI but the switching duty and conduction loss were less for proposed FSILI. DC bus utilization was further improved with Third harmonic Injection PWM.
- A grid integration algorithm with active power control at unity power factor was proposed and the Novel FSILI topology was integrated to the utility grid to investigate the grid control capability. For different power levels active power injection was carried out and the harmonic content of the injected current was found to be within the IEEE standards.
- Islanding mode of the Novel FSILI with current control was also carried out to analyze the standalone operation of the inverter with similar current control. THD is found to be within limits. Transient response under current control operation also investigated with proposed current control method.

8.4. Limitations and Future Works

Here the proposed FSILI is investigated for grid control operation with active power injection only. Further with some modifications in the control algorithm the reactive power control can be implemented. Also, with the bidirectional power flow capability of the FSILI, it can be used in the V-G and G -V operation .Under normal operation of the inverter V to G mode will be there and with appropriate charge control circuit, from grid to vehicle (Battery charging) operation can also be done. To the input side of the inverter, some renewable sources can be connected and the operation under

maximum power point tracking can also be investigated. The proposed topology can be used in series and shunt compensation of electric grid. With the high quality AC output and with ease of control and implementation the proposed Novel FSILI will find more applications in the future.

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List of Publications

Journal Publications

1. **K. T. Ajmal**, K. Muhmmadali Shafeeque, B. Jayanand, "A Novel Four Switch Infinite Level Inverter", ***Journal of Circuits, Systems and Computers*** ***Vol.29,No. 12 (2020) doi:10.1142/S02181266205(SCI)***
2. **K. T. Ajmal**, K.Muhammadali Shafeeque, B.Jayanand, "A Modified Current Controlled Novel Infinite Level Grid Tied Inverter" ***International Journal of Electrical Engineering and Education*****(SCI)** (Under Review)

Conference Publications

1. **K. T. Ajmal**, S. K. Muhammadali and B. Jayanand, "A Modified Three Phase Infinite level Inverter with Improved DC Bus Utilization,"***5th International Conference on Communication and Electronics Systems (ICCES),*** Coimbatore, India, 2020, pp. 26-32, doi: 10.1109/ICCES48766.2020.9137913.