A New DC-DC Converter based Infinite Level Inverter (ILI) for Distribution STATCOM

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By

Renukadevi V

Under the guidance of

Dr. Jayanand B.

Department of Electrical Engineering

Government Engineering College, Thrissur – Thrissur

University of Calicut

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Department of Electrical Engineering
GOVERNMENT ENGINEERING COLLEGE
THRISSUR- 680009

Certificate

This is to certify that the thesis entitled ***"A New DC-DC Converter based Infinite Level Inverter (ILI) for Distribution STATCOM"*** *is the record of bonafide research work done by* ***Ms. Renukadevi V.*** *under my supervision and guidance at Department of Electrical Engineering, Govt. Engineering College, Thrissur in partial fulfillment of the requirements for the Degree of Doctor of Philosophy under the Faculty of Engineering, University of Calicut.*

Thrissur-9 ***Dr. JAYANAND B***

11.02.2019

DECLARATION

I Renukadevi V. *,hereby declare that the thesis entitled* ***"A New DC-DC Converter based Infinite Level Inverter (ILI) for Distribution STATCOM"*** *is based on the original work done by me under the guidance of* ***Dr. Jayanand B****, professor, Department of Electrical Engineering, Govt. Engineering College, Thrissur for the award of Ph D programme under University of Calicut. I further declare that this work has not been included in any other thesis submitted previously for the award of any Degree, Diploma, Associateship or Fellowship or any other title for recognition.*

Thrissur-9 ***Renukadevi V.***

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Thrissur - 9 ***RENUKADEVI V.***

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Abstract

Multilevel Inverter (MLI) topologies are widely used in the field of industrial applications such as large motor drives, flexible AC transmission systems, power quality improvement devices, renewable energy converters and so on to reduce harmonic content in the output voltage. The operation of these inverters ensures some inherent benefits over conventional two-level inverters. Improved quality of output voltage of the multilevel inverters is one of the most significant advantages. But the number of switching devices increases with every increase in the output voltage level. Although there are a lot of works available in literature to reduce THD, to improve the switching angle and the switching pattern of the multilevel inverters and to reduce the switching loss, little attention has been paid to improve the dc-link utilization. In this thesis, the use of a new three-phase infinite level inverter topology as DSTATCOM is proposed. The heart of this switched mode dc-ac inverter is a high frequency operated dc-dc buck converter stage at the front end followed by a power frequency operated H-bridge. The duty ratio is varied in a rectified sinusoid manner. This topology uses a minimum number of switching devices for an infinite number of output voltage levels. The number of voltage levels of an ILI depends on the carrier frequency used. THD profile of output waveform from FFT analysis of ILI shows that the THD is less than 2% and maximum individual order harmonic is less than 0.4 % of the fundamental, for a switching frequency of 10 kHz. With the advent of Wide Band Gap Devices, the frequency of operation can be increased to mega hertz levels, thereby achieving perfect sinusoid. Its reduced harmonic content and high dc-link utilization outweigh other inverter topologies and switching techniques.

The main focus of this work is to use this newly developed ILI for harmonics and reactive power compensations at load side. The synchronous reference frame (SRF) strategy is used in this work to generate current reference for distribution static compensator (DSTATCOM) and fixed band

hysteresis current controller is used to inject reference current generated, at the point of coupling. The design, modeling and simulation of three-phase infinite level inverter are carried out in Matlaab/simulink environment. The performance of newly introduced topology has been validated with different load conditions. To validate the feasibility of three-phase infinite level inverter topology, a laboratory prototype is developed and its good dynamic performance is validated. The compatibility of ILI is verified for DSTATCOM applications through simulation, hardware implementation and analysis.

Since photovoltaic generation units are a crucial part of future power systems, an attempt has been made to incorporate the photovoltaic energy for this study and its performance as PV-DSTATCOM using this three-phase ILI is analyzed.

The main objectives of the research can be enumerated as follows.

- To analyze various inverter topologies used for DSTATCOM applications.
- To develop a new dc-dc converter based infinite level inverter (ILI) which has reduced switching loss, low dc-bus voltage and fast dynamic response for power quality enhancement.
- To exploit the features of the newly developed infinite level inverter (ILI) to develop a distribution STATCOM.
- To control current harmonics and reactive power of distribution system using this ILI with photovoltaic system as dc source.

The first phase of the research work is concerned with the comparative study of voltage source, current controlled PWM multilevel inverters employing hysteresis current controllers that are applied to improve power quality in distribution network via reactive power control and harmonic filtering. Performance of DSTATCOM using these inverter topologies is analyzed theoretically and the performance of classical two level three-phase voltage source inverter based DSTATCOM is verified through simulation. Two types of current reference extraction schemes have been explained and compared.

Modeling, design and analysis of new three-phase infinite level inverter have been done as the second phase of the work. This switched mode dc-ac inverter consists of a high frequency buck converter stage at the front end, followed by a low frequency H-bridge. This inverter topology can generate voltage levels of any number depending upon the carrier frequency used in the buck

converter stage with the same number of circuit components. This is achieved with a sinusoidally varying duty ratio with a constant dc voltage. Fully rectified SPWM technique is used as control logic for implementing sinusoidally varying duty ratio. Only three high frequency switches are required to realize a three phase ILI. This reduces the switching losses substantially. The proposed topology has been compared with traditional inverter typologies, and it is proved that a three phase ILI requires the least amount of DC source voltage for generating 400 V rms value of fundamental line voltage. The ILI requires only 325 V as dc bus voltage. Increasing the number of levels in output voltage waveform reduces harmonics to a greater extent. THD profile of voltage waveform from FFT analysis of ILI shows that the THD is very less.

The third phase of the research work concentrates on the implementation of DSTATCOM using the three-phase infinite level inverter topology. The significance of the proposed system is the incorporation of three-phase ILI onto DSTATCOM which brings in all advantages of ILI into reactive power control. SRF strategy has been implemented in hardware using three-phase ILI topology and results obtained validate the system capability of high dc bus utilization. The experimental results are presented to verify the analysis and demonstrate the feasibility of the proposed system. In addition to this, modeling and simulation of three-phase ILI to control the reactive and harmonic current of the photovoltaic fed distribution network (PV – DSTATCOM).

The ILI-DSTATCOM with a single PI controller could achieve the functionalities of reactive power control and harmonic filtering. The dc-link capacitor of the system is used to supply reactive power. The results show that reactive power compensation is accomplished with SRF strategy and it does not put much stress on the dc-link capacitor. With a single PI controller, the system operates in all the possible modes with lower THD, reduced losses, and lower dc-link voltage. The overall setup is found effective in controlling the reactive power along with harmonic filtering.

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Chapter 1
Introduction

Industrial revolution has revolutionized human life with enhancements in modern technologies. The main contribution to the industrial advancements is owing to the availability of electrical energy that is distributed via energy utilities across the world. The notion of power quality in this context is booming as a “Basic Right” of consumer for safety as well as for interruption free operation of end equipment. The electricity customers whether domestic or industrial, need power, free from glitches, distortions, flicker, noise and outages.

The power quality issue and the power quality compensation concept have been there from the moment the power industry got established. Earlier, reactive power compensation was the only concern. Since most of the industrial loads being highly inductive, power was wasted unnecessarily at the generation, transmission and distribution systems. However, with the arrival of both electronic and power electronic loads, harmonics also added to the existing issue. While reactive power leads only to losses, the problem due to harmonics is worse. By absorbing harmonic currents, loads distort the supply voltage and make them deviate from their sinusoidal nature. Further, they devastate the existing reactive current compensation systems like capacitor banks. These problems have lead to the invention of better systems that can compensate for both reactive and harmonic currents. There are several solutions to improve power quality such as fixed capacitors, switched capacitor banks, synchronous condensers, static VAR compensators, converter based flexible AC transmission systems (FACTS) or active power filters (APFs). Among all, the converter based FACTS were the outcome of continuous research in this direction and they aid to achieve dynamic compensation of reactive and harmonic currents required by the load.

In the electrical system, massive utilization of nonlinear loads in the industry as well as domestic sector results in the generation of harmonics and disfigures load current waveform. This further produces current harmonics in load side and they tend to flow to the source through Point of Connection (PoC). These current harmonics additionally gives rise to

voltage harmonics on the source side which cause disturbance to nearby costumers. Thus, it is advocated to control the current harmonics on the load side.

Improvisations in reliability, power density and efficiency have been the key concern in the recent research advances of inverter topologies. Voltage Source Inverters (VSIs) are the most popular dc-ac power converters utilized in power electronic systems. The VSI embraces only the buck capability with the inversion stage, i.e., the output ac voltage never exceeds the dc input voltage. This however is not a problem for a number of applications with high dc bus. But numerous applications need the output ac voltage that is higher than the input dc supply. In traditional bridge-type inverter, the two switches of the same leg cannot be turned-on simultaneously otherwise the inverter will be short circuited and damaged. So a dead time needs to be set between the driving signals of the two switches. Compared to the traditional bridge inverter, the existing dual-buck-type inverters require two or more inductors, which in turn increase the inverter volume and weight. Even if the methods of inductive coupling, magnetic integration, and divided inductor are adopted in dual-buck-type inverter to decrease the volume and weight of magnetic device, still the volume and weight have not been reduced less than that of a single inductor multilevel inverter topology. There are three major types of multilevel inverter topologies: Diode-Clamped, Flying-Capacitor or Multi cell, and cascaded H-bridge. These topologies are suffering from complex circuit structure and need large number of power devices so that the control and triggering circuits have become complex.

The main significance of multilevel inverter is that the voltage stress is reduced during each switching operation thereby reducing the switching loss and corresponding increase in power efficiency. But, the number of switching devices used in multilevel inverters is more than that used in the conventional topologies. Consequently, its control and circuit realization are more complicated. In many electrical dc-ac power conversion applications, the ac output voltage requirement is higher than the input voltage. If a voltage source inverter (VSI) is used, then an additional dc-dc boosting stage is needed to overcome the step-down VSI limitations. Recently, several impedance source converters are gaining greater attentions as they are capable of providing buck boost capability in a single conversion stage. An inverter topology which can address the above mentioned limitations of existing topologies can be of significant interest in the area of power electronics and power system since a reliable and efficient system which produces minimum THD can be put into use in various applications.

In this research work, a new inverter topology named three-phase infinite level inverter (ILI) topology is discussed.

Infinite level inverter (ILI) topology is basically a switched-mode dc-to-ac inverter comprising of a dc-to-dc converter and H-Bridge. ILI configuration has many advantages over the traditional bridge type inverter. Only one switch operates at high frequency and as a result, switching losses will be significantly less. This makes operation at high frequency feasible. The number of voltage levels in open loop depends on the frequency of carrier wave. Also the fundamental output voltage obtained from the proposed ILI requires less input dc bus voltage and thus very high dc-link utilization is possible. The significance of this topology is that only three high frequency switches are required to realize the three-phase ILI. This reduces the switching losses substantially.
The power quality sector is strong and aggressive. To build competitive new products, many design constraints including cost and size reduction, reduced power consumption, power factor correction, and reduced THD must be addressed. In order to overcome these challenges, advanced technologies and power electronic systems are necessary.

The motivation of the research and objectives are presented in section 1.1. The scope of the research is explained in section 1.2. The organization of the thesis is briefed in section 1.3

1.1. Motivation of the Research

Various researches on power electronics focus to develop multilevel inverter topologies with reduced switching elements and passive components. Voltage levels and characteristics of the waveform are transformed with different inverter techniques. Each inverter technique has its own limitations regarding various constraints such as number of elements used, stresses on switching devices and efficiency of inverter topology. Many of these inverters have emerged in industry for a number of applications. Nowadays, efficient power conversion is more significant than ever before owing to the power quality constraints. Efficient operation of converter topologies is also significant in the cases of alternative energy resources such as fuel cells, photovoltaic energy, wind energy and ocean wave energy which need proper power conditioning to adapt to different types of loads. Furthermore, the entire area of electrical power systems is still demanding for new power electronic inverter techniques in order to determine the more efficient and cheaper ways to achieve quality power.

In the beginning, conventional voltage sourced inverters and current sourced inverters were used for power quality enhancement. In recent years, multilevel inverter topologies have emerged as powerful tools capable of overcoming the issues with classical inverters. To improve the performance in various critical situations, a number of modifications of these topologies have been presented in various literatures for distribution side static compensation applications. Some structures are more complex than others and control methods used are also not very accurate, reliable and flexible with respect to power quality analysis. In the literature, researchers have attempted to implement efficient multilevel inverter topologies and control techniques for power quality improvement under practical constraints. However, as the number of voltage levels increases, number of switching devices and number passive elements also increases. This issue is a key motivation for the present work.

Different methods of extracting current reference are also surveyed in the literatures. Since clean, reliable and high quality power is one of the major concerns in today's world, power electronics will definitely play a vital role in filling this gap. The extensive literature review on reactive power compensation and harmonic filtering has further motivated for analyzing the limitations of classical voltage source inverter topologies based DSTATCOM. The reduction in dc-link voltage requirement and hence the size and type of dc-link capacitor, reduced switching losses, avoiding shoot through problems are also the points of interests to be investigated.

1.1.1 Objectives

The objectives of the research can be listed as follows:

- To analyze various inverter topologies used for DSTATCOM applications.

- To develop a new dc-dc converter based infinite level inverter (ILI) which has reduced switching loss, low dc-bus voltage and fast dynamic response for power quality enhancement.

- To exploit the features of the newly developed infinite level inverter (ILI) to develop a distribution STATCOM.

- To control current harmonics and reactive power of distribution system using this ILI with photovoltaic system as dc source.

1.2 Scope of the Research

Pulse width modulated voltage sourced converters (PWM-VSC) have several merits over the conventional bridge type converters. But there are a few issues related to this type of converters. For high power and voltage ratings, device constraint as well as high switching loss generates severe issues. Different pulse width modulation techniques such as sinusoidal, 3rd harmonic injection and space vector PWM (SVPWM) employ high frequency switching to attain quality output voltage with less ripple. Increasing number of voltage levels in a multi-level inverter requires an increase in number of semiconductor switches and passive components. The issue of dead time requirement and shoot through in PWM converters distorts the output waveform and transfers less energy to load. Here is the gap.

A three-phase VSI called three-phase Infinite Level Inverter (ILI) is presented to eliminate all the above mentioned issues to a great extent. The device constraint and switching loss at high frequency is substantially minimized owing to reduced input dc voltage. To get same output voltage, the suggested inverter needs only 50 % of the dc-bus voltage compared to sine PWM inverter.

The scope of this thesis can be listed as follows:

In this ILI, only three switches operate in the carrier frequency and the remaining twelve switches operate in fundamental frequency. Thus switching loss is reduced substantially.

- The new topology can efficiently replace existing multilevel topologies and the application can extend in all areas of conventional inverter application.

- This ILI is used for the realization of a DSTATCOM.

- ILI based DSTATCOM can be employed in critical application area such as hospitals and airports as it complies with IEEE 519 standard.

1.3 Organization of the Thesis

In this thesis, an infinite level inverter based DSTATCOM system with synchronous reference frame strategy to produce current reference and fixed band hysteresis current controller to provide reactive power compensation and harmonic current elimination is presented. Reactive power compensation and harmonics elimination are achieved by maintaining a low dc voltage in the dc side. Unity power factor is achieved at the point if

coupling. This ILI consists of only three high frequency switches. This system enhances the power quality in terms of lower THD, reduced losses and efficiency. Both simulation and experimental results are presented to validate the system. Results also show the improvement in power quality of a PV supported distribution network.

The chapters of the thesis are organized as follows:

The literature review regarding the existing power quality disturbances, solutions and various inverter topologies used for DSTATCOM applications are explained in Chapter 2. Chapter 3 presents simulation analysis of conventional voltage source inverter based DSTATCOM with two current reference extraction methods. Derivation of SRF strategy and IRPT algorithm are also presented in the same Chapter. A detailed explanation of the theory, circuit, and design of three-phase ILI model is demonstrated in chapter 4. The explanations of THD and current and voltage characteristics are subsequently discussed. Chapter 5 deals with the operation of the ILI as three-phase, three-wire DSTATCOM and its power quality compensation performance. Chapter 6 explains how the infinite level inverter operates in PV supported distribution network and the compensation for reactive and harmonic currents. This is followed by the explanation of the methods of hardware implementation of the three-phase ILI based DSTATCOM using SRF strategy and fixed band hysteresis current controller in Chapter 7. This includes the design and implementation of various control circuits, sensors used and calculation of reference currents and so on. The hardware results of ILI based DSTATCOM performance has been presented in this chapter. Analysis of experimental results demonstrated in this Chapter shows the effectiveness of the system. Also the results of low power prototype presented in the Chapter helps to validate these concepts. The last Chapter presents the performance of ILI as PV-DSTATCOM with SRF method to extract reference currents. Along with the fixed band hysteresis current controller, the source voltage and current are in-phase with each other and also effectively compensate for harmonic and reactive currents. Results and analysis of various modes of operation of the system are done using MATLAB/Simulink. Chapter 8 concludes the research work. Salient features of the proposed DSTATCOM inverter have been given in this Chapter. Suggestions for future work are also presented.

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Chapter 2
Literature Review

2.1. Introduction

The electrical networks have been polluted with the proliferation of nonlinear loads that cause undesirable effects [1] such as poor system efficiency and low power factor (PF). They also cause disturbance to other customers and interference in nearby communication systems. Nonlinear loads like personal computers, fax machines, uninterruptable power supplies (UPSs), television sets (TVs), microwave ovens, air conditioners etc lead to current/voltage harmonics generation and absorb reactive power. Huge reactive current in power systems is one of the most important power quality issues that increases transmission losses and lowers the stability of a power system [2]–[20]. Reactive power compensators are an important remedy to this problem. The detrimental effects of harmonics are another major concern for researchers these days. So, numerous efforts have been made to conquer the harmonic current in the utility. Traditionally, shunt passive LC filters have been used to mitigate the current harmonics, and power capacitors are used to enhance the PF of the system. Yet these filters have the disadvantages of fixed compensation, huge size and can also excite resonance conditions [21]. The sensitivity of these issues also has attracted the attention of researchers to develop techniques with adjustable and dynamic elements.

Different types of power quality enhancement solutions are reviewed in section 2.2. The various FACTS devices for reactive power compensation and harmonic filtering are reviewed in section 2.3. The converter circuit is the most significant part of the compensation system. The various inverter configurations for DSTATCOM are briefed in section 2.4 and the converter control strategies for DSTATCOM are discussed in section 2.5 and the review is concluded in section 2.6.

2.2 Power quality enhancement solutions – a review

- Fixed capacitors
- Shunt reactors
- Synchronous condensers
- Static VAR compensators
- Converter based FACTS or active power filter

The above mentioned devices are used as the reactive power compensation devices. These devices either draw or supply reactive power to achieve the desired reactive power balance. The following sections discuss the principle behind each of the above solution strategies

2.2.1 Fixed capacitors

The traditional way of improving PF is by the utilization of switched parallel capacitors. The disparity of load and different voltage profiles over a day result in vast variations in the reactive and harmonic VARs absorbed by the plant. Almost all utilities adopt switched shunt capacitor banks to enhance the power factor near to unity. Capacitor banks are incrementally switched in by electromechanical switchgear to keep the required power factor. Switching of a capacitor bank using electromechanical switchgear can introduce transients. This can be overcome by thyristor-switched condensers to control the turn-on angle and the inrush current. The usage of fixed capacitors were the first attempt for reactive current compensation and are connected in shunt for reactive power compensation thereby ensuring acceptable voltage levels in heavily loaded conditions. Suitable sized capacitor banks are applied to bus directly or to the transformer tertiary winding. When a condenser is connected in parallel, the voltage at the point of connection (PoC) forces a constant leading current to flow. This compensates for the lagging current absorbed by the load. These are a convenient method of retaining bus voltages within the limit and are distributed along the system to minimize losses and voltage drops [22].Obviously, the disadvantage is that the leading current drawn is fixed by the PoC voltage and when the load is varying, there will always be improper compensation. The switched capacitor banks also have issues with source–sink resonances which need the use of detuning reactors [23].

2.2.1.1 Series capacitors

Condensers connected in series with line reduce the net reactance of the network [24].So, the ability to exchange power is increased and it lowers the imaginary power demand of the system. Also, series capacitors allow economical loading of long transmission lines. But its usage is restricted owing to the problem of Sub Synchronous Resonance (SSR) [25].

2.2.2 Shunt reactors

The parallel connected reactors are used to balance the effects of line capacitance [26]. Under light loaded conditions, these reactors are used to avoid over-voltages. In case of undesirable voltage rises they are activated in order to check voltage rise. In fact, it is not a counter action taken to eliminate voltage collapse. During heavy loaded situations, they may have to be disconnected.

2.2.3 Synchronous condensers

The grid connected synchronous machines with controlled excitation of field [27] can be used to absorb or deliver reactive current. It is represented as a variable voltage source in series with a reactance. Unlike the capacitor based compensation, the synchronous condensers are dynamic. However, it is subjected to some demerits like slow response to varying load conditions due to the inertia of mechanical parts of the machine and cannot be used for compensating harmonic currents absorbed by the load. Even though it has certain advantages over fixed and switched capacitors, synchronous condensers are hardly chosen because of its huge installation and running cost. It is capable of modifying the output reactive power to preserve fixed terminal voltage by a voltage regulator. They are chiefly connected to transformer's tertiary windings. Some of the merits are as follows;

- It can be controlled to follow the reactive current requirement of the system
- The reactive current compensation is not fixed entirely by the PCC voltage (though PCC voltage also influences it)
- It can provide both lagging and leading reactive currents

2.2.4 Conventional Static Var compensators

Conventional Static Var compensators (SVCs) are utilized for the dynamic compensation of reactive currents as the loads vary over a day results in vast change in the reactive and harmonic VARs absorbed by the plant. Static Var Compensators (SVCs) use power electronics for power quality compensation. The compensating system can be controlled to follow the reactive power requirement of the load by controlling the thyristors and are affixed in parallel with the buses whose phase voltages are to be controlled. This system is preferably convenient for applications where voltage control should be directly and quickly performed and are optimally placed in a line to maximize the loading limit. Its major disadvantage is that the compensating system itself will inject harmonics into the system due to switching action. Additionally, it suffers from resonance issues and slow response [3-4].

These traditional approaches tend to be less optimal and less profitable because of their cost and bulky construction. In the developing utility environment, financial and market issues require a more optimal and profitable performance of the power network regarding generation, transmission and distribution. To obtain both operational reliability and financial profitability, it is evident that more efficient utilization and regulation of the existing electrical system infrastructure is necessary. Conventional ways of upgrading the system infrastructure in the form of new transmission or distribution networks, substations, and associated elements have proven to be extremely difficult, highly expensive, time-consuming and controversial. These aspects have given rise to innovative technologies to improve power systems with more efficient systems management.

2.2.5 Converter based FACTS or active power filter

The various compensation techniques discussed so far are applicable in the system only in the absence of harmonics. With the advent of harmonic loads, there are some problems with the capacitor based compensation methods such as heating of capacitors due to large harmonic current flow and failure due to resonance phenomenon. The harmonic current compensation is also a burden for synchronous condensers and SVCs. The active power filters (APFs) were

developed to overcome the demerits associated with SVCs and compensating for reactive current with quick response, reduced harmonic current injection, and improved performance [5]–[10].

On the basis of how the filters are connected, active power filters (APFs) are categorized into four types:1) shunt [28], 2) series [29], 3) series–shunt [30], and 4) hybrid [31]. Owing to the limitations of classical passive devices, APFs have been attracted the attention over the past few years because of their benefits such as small size, the capability of compensating both harmonic currents and reactive power and avoiding resonance conditions with the system. In contrast, the active power filter with high switching frequency and high bandwidth dc to ac inverter is costly to implement. In a practical system, significant cost and complexity are encountered.

The major benefits of utilizing FACTS devices are [33];

- Improved utilization of existing network
- Enhanced system reliability and availability
- Improved dynamic and transient grid stability and minimization of loop flows
- Improved quality of supply for sensitive loads
- Environmental benefits

Constructing new transmission or distribution networks to meet the escalating demand of electrical power is always limited economically and by environmental constraints. There exists a scope for effective utilization of existing electrical system assets by incorporating FACTS devices [34]. FACTS devices increase transmission system reliability and capability by mitigating the influence of faults and by lowering the number of outages. They can stabilize the electrical systems along with imparting greater ability to transfer energy and reduced risks of line trips. Thus increase in the dynamic and transient grid stability and minimization of loop flows are attainable. Furthermore, they are environmental friendly devices as they neither consists of harmful materials nor generate waste or pollutants. In fact, FACTS devices help to distribute electricity more economically by effective utilization of existing networks thereby lowering the requirement for additional distribution networks.

FACTS controllers are power electronic based apparatus that are utilized for the dynamic control of voltage, impedance and phase of medium to high voltage AC lines. There are two types of FACTS controllers; thyristor-based and converter-based. Thyristor-based FACTS devices use traditional thyristors to regulate voltage, impedance, and angle. Static Var Compensator (SVC)

[32], thyristor-Controlled Series Capacitor (TCSC), and the thyristor-Controlled Phase Angle Regulator (TCPAR) are the examples of thyristor-based FACTS devices. The classical thyristor-controlled compensators, the SVC and TCSC, present variable reactive impedance to the network [35]. The SVC operates as a controlled shunt reactive admittance that generates the necessary reactive compensating current. Thus, the achievable reactive compensating current is a function of the prevailing line voltage.

The converter-based FACTS devices employ self-commutated, voltage-source switching converters (VSSC) to realize rapidly controllable, static, synchronous AC voltage sources. This approach can provide reactive compensating shunt current that is independent of system voltage, as well as a series reactive compensating voltage that is independent of line current. They can also exchange adjustable real power with the ac system while providing independently controllable reactive power compensation. Indeed, they provide all the required characteristics needed for comprehensive real-time system management and hitherto unattainable utilization of system assets. Using FACTS, the present electrical system operation has been improved with a minimum investment of infrastructure, minimum environmental impact, and less construction time compared to the construction of new power lines.

2.3 Types of FACTS devices

Depending on the way of connection, FACTS devices are classified as follows;

- **Series -** Dynamic Voltage Restorer (DVR) which is a series active filter that helps to keep rated voltage at the terminal of sensitive loads so that the load does not malfunction due to variation in voltage [36].
- **Shunt -** Static Synchronous Compensator (STATCOM) which is a parallel filter which improves the power factor and voltage at the point of common coupling (PCC) and reduces the current harmonic content injected into the source side by injecting current.
- **Combination of series and shunt –**Unified Power Quality Conditioner (UPQC) which is a parallel-series filter to maintain required voltage at load end, while maintaining the power factor and harmonics injected to the grid as per requirement [37].
- **Static Var Compensators** (SVC's) – SVCs are the most important equipment in the FACTS family. They provide vast range of control, quick response and better range of reactive power capability. Also, SVCs are utilized to dampen power swings, to enhance

transient stability and to minimize system losses by optimized reactive power regulation [32].

- **Thyristor Controlled Series Capacitors** (TCSC) – It is an extension of traditional series capacitors by adding a thyristor-controlled reactor. Connecting a controlled reactor in shunt with a series capacitor enables a continuous and flexible series compensation system. This combination improves energy transfer, dampening of power oscillations, dampening of sub synchronous resonances (SSR) and control of line power flow [35].
- **Unified Power Flow Controller** (UPFC) **–** connection of a STATCOM with a series branch in the transmission line through its dc circuit results in a UPFC and its merits are of the combination of a STATCOM and SSSC [38].

STATCOM connecting to distribution system and operating for the mitigation of the multiple power quality problems associated with distribution network is known as Distribution STATCOM (DSTATCOM). The DSTATCOM is a mature technology for providing the reactive power compensation, load balancing and neutral and the harmonic current suppressions in the distribution networks [33]. It also used to control the terminal voltage, suppressed voltage flickers and improving the voltage unbalance of the three-phase systems. Classical methods of utilizing power capacitors and the static VAR compensator using TCR and TSCs have been used to eliminate some of these problems. But, the DSTATCOM technology is regarded as the best technology to eliminate the current-based power quality problems and thus it is being used frequently in FACTS devices. DSTATCOM is categorized into three types: single-phase two wire, three-phase three-wire and three-phase four-wire systems. This work deals with the three-phase DSTATCOM.

2.4 Inverters for DSTATCOM

2.4.1 Current Sourced and Voltage Sourced Inverters

The inverter is the most important element of the distribution STATCOM system and presently different inverter topologies are reported in the literature. Based on the type of inverter, these are mainly categorized into two types namely voltage source inverters (VSIs) and current source inverters (CSIs). Voltage source converters (VSCs) are the most prevalent and widely accepted for DSTATCOM over current source converters (CSC) as it is lighter, cheaper and can

be easily expanded to multilevel inverter topologies to enhance their rating and efficiency and to reduce the switching frequency that is very crucial factor in design and implementation of the STATCOM. In addition to this, VSI structure is more economical in terms of component cost and availability. A CSC is normally more reliable and fault tolerant than a VSI because of the high series inductor that limits the rate of rise of current in the event of a fault. On the contrary, it acts as a nonlinear current source that generates nonlinear current or demand for reactive current by the load. CSIs are considered as reliable structure for STATCOMs but they are bulkier than VSI as it consists of inductors. It also generates larger losses and needs large value of shunt capacitors. Furthermore, they cannot be used in multilevel inverter modes.

The DSTATCOM system based on classical voltage source inverters (VSIs) have emerged as the most effective solution for VAR compensation over the conventional thyristor-based compensators (i.e., Static VAR Compensator) owing to their feasibility, superiority and capability to compensate for a vaster range of VAR in very short time [39]. However, for satisfactory performance of STATCOM, it is necessary to maintain a higher dc-link voltage. Generally, much higher value than line voltage for a three-phase three wire system that leads to increased inverter rating, makes the inverter heavier and requires higher voltage rating of insulated gate bipolar transistor (IGBT) switches which further increase the size, weight, and cost of the system. Additionally, VSI based DSTATCOM system use a large L-type interfacing filter to shape the injected currents. It generates a high voltage drop across it that further increases the need for a larger value of the dc-bus voltage for necessary compensation [40].

2.4.2 Advantages and disadvantages of classical two-level VSI

Advantages

- Standard PWM methods can be used.
- Less number of power circuit elements as compared to other inverter circuits.
- Redundancy can be incorporated to enhance reliability by utilizing more series elements than actually required

Disadvantages

- When the switch is in OFF condition, the whole dc supply voltage appears across each switch and is greater than the voltage rating of the independent devices.
- In the OFF state, the voltage sharing between the devices is not automatic due to the difference in the leakage currents. High shunt resistors to be used to conquer this static sharing problem.
- Owing to the variations in the speed of switching, the devices will not share the voltage during switching. Special gate drive techniques and special snubber circuits to be incorporated to acquire dynamic sharing.
- Higher switching frequency results higher harmonic content in the output voltage.

From the above discussion, it is evident that the traditional VSI have many disadvantages than advantages. So, an alternative solution to meet the high power demand is adopting multilevel inverter concept.

2.4.3 Multilevel Inverter topologies

The basic voltage sourced inverter configuration is a 2- level inverter as it can produce the output voltage of + V and - V. However, there are a number of inverters that are capable of generating large number of output voltage levels by arranging several dc sources and switching devices in the suitable manner. They are known as multilevel inverters (MLIs). These dc sources can be renewable energy sources, ultra-capacitors, fixed dc sources and so on. MLIs perform power conversion better than two-level VSIs with the benefits of high voltage/power capability, reduced distortion in the waveform, and improved efficiency [41]. The multilevel inverters start from three levels. With these type of inverters, as the number of levels increases, the total harmonic distortion (THD) decreases. An output voltage with low THD is highly desirable factor in terms of power quality. As the number of levels approaches infinity, the THD approaches zero. But the number of voltage levels is limited by voltage imbalance issues, voltage clamping requirement, circuit layout and stacking constraints (Nabae et al 1981).

In recent past, MLIs are largely incorporated in a medium voltage grid as they can overcome the problems associated with single semiconductor switching device connecting directly to the grid

and hence these are used as an alternative for medium and high power applications. Nowadays, multilevel inverter (MLI) topologies are widely accepted as a solution to power quality (PQ) related issues like reactive power compensation on transmission and distribution networks (i.e. STATCOM) and an interface inverter for renewable energy resources such as solar, wind, fuel cell etc. The power quality of the electrical system is affected by the harmonics produced by the nonlinear loads. Multilevel inverter enhances the power quality by performing the power conversion in small voltage steps. The traditional two-level, three-phase voltage source inverters are largely replaced by multilevel inverter technology due to its superior performance like lower switching stress and lower THD. Multilevel inverter can boost the power handling capacity by (m-1) times than that of two-level inverter by cascade and shunt connection of power semiconductor switches. It can abolish the low order harmonics from the output waveform and can reduce the electromagnetic interference (EMI) as it compares with the two level inverter systems with same power handling capacity. Furthermore, MLIs have proven their capability to overcome issues associated with the classical two-level inverters for STATCOM implementation and therefore have conducted an extensive research in the last few decades. There are different topologies of multilevel inverters that have been proposed and demonstrated in the open literature [42]. The use of MLI topologies reduces size, weight, and cost as it can avoid line frequency transformer.

2.4.4 Advantages and disadvantages of multilevel inverters

Advantages of MLIs

- MLIs can operate at both fundamental and high switching frequency, so that efficient performance and reduction in switching losses can be achieved.
- They can enhance power quality and dynamic stability of the system.
- Low switching stresses and electromagnetic interference (EMI).
- Owing to their simple and modular structure, they can be stacked up to an almost unlimited number of levels.
- They are an ideal interface between the grid and renewable energy sources (i.e. PV or fuel cells).

Disadvantages of MLIs

The main demerits of employing MLIs are given below;

- Requirement of huge number of capacitors.
- The number of switching devices increases with the number of voltage levels.
- Problems in achieving capacitor voltage balancing.
- Complication in control as the number of passive and active elements increases

2.4.5 Types of MLIs

The major configurations of MLIs are divided into three topologies [7], [43], [47] [48] [50]: Neutral point clamped (NPC) or diode clamped multilevel inverters [38], [47], Flying capacitor (FC) or capacitor clamped multilevel inverters, and Cascaded H-bridge (CHB) multilevel inverters [6], [9], [48]. Among all these MLI topologies, the cascaded H-bridge multilevel inverter (CHMLI) has been an attractive topology for DSTATCOM system due to its modularity, extensibility, and control simplicity [43]–[45]. The CHB topology is also principally attractive as it needs the smallest hardware to produce the same voltage levels. Furthermore, owing to its flexible structure, implementation, maintenance, and upsizing of MLIs are not complicated [46].

2.4.5.1 Neutral Point Clamped (NPC) Multilevel Inverter (Diode Clamping)

Neutral point clamped (NPC) inverter was initially suggested in 1981 by Nabae et al. [49]. It was considered as the first type of multilevel inverters and is the most commonly used MLI topology, known as the 3-level NPC inverter. Figure 2.1 shows a three-level NPC MLI topology. It is the modification of the traditional two–level voltage source converter (VSC). It consists of two additional switching devices in each leg of conventional VSI and the two diodes connected in series between the lower and upper end of common neutral point‘0’are clamping diodes that help to clamp each switch voltage. In this topology, each switch tolerates the voltage of Vdc / 2 and each switch pairs working as complimentary fashion. So, the dc-link voltage of 2 Vdc can be acquired if these devices have the same characteristics than the switches in two-level one. The capacitors C1 and C2 share the dc-link voltage equally. Thus, there is no requirement of an additional dc source. Over the past three decades, these inverters have been successfully utilized in industries for the power quality compensation. To support a higher operating voltage and

power, this converter topology can be easily extended to higher voltage levels. In this technology, the dc-bus capacitors are used to provide the temporary energy storage during switching actions to distribute reactive power among the phases and to support the system losses.

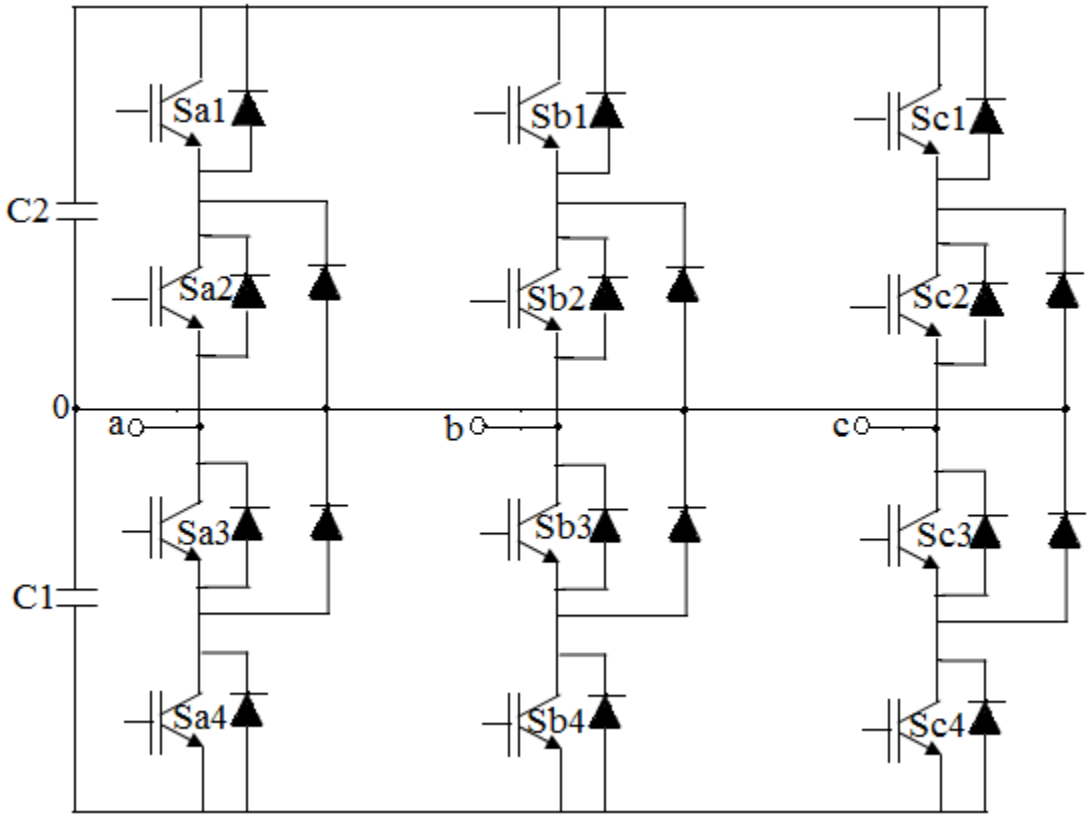


Figure 2.1 Three-level NPCMLI

The doable switching pattern for a three-level NPCMLI is given in table 2.1. As shown in the table, there are only three feasible switching patterns for the three- level NPCMLI. Other switching possibilities create serious issues like short-circuit in some dc-bus capacitor or they do not provide any current path at the output. For example, consider the switches S1, S2 and S3 are ON, the capacitor C2 will be short circuited. Even though theoretically it is possible to increase the number of voltage levels, the application of NPCMLI is limited to five levels because of the complexity of the system, entanglement of the control and a huge number of elements needed [50]. Another restricting factor in the number of levels in NPC inverter is demonstrated by the unequal distribution of semiconductor losses among the switching devices that restricts the operating frequency and the output power. The later can be overcome by incorporating extra

semiconductor devices in shunt with the clamping diodes called Active Neutral Point Clamped (ANPC) MLI. This topology also has the problem of power loss and the requirement of more power electronic devices that lead to an increase in the complexity of the entire system. Another important thing is that NPCMLIs do not provide a modular structure so that cascading of power semiconductors is required to attain the desired voltage levels for grid connected applications is not possible. It is also important to mention that the reverse recovery diode is an important challenge in the design of NPC type MLI topologies. Although the NPCMLI topologies face the above mentioned restrictions, the three-level NPC topology has been successfully implemented as STATCOM [51].

Table 2.1 Doable switching configurations for three-level NPCMLI

S1	S2	S3	S4	Phase-Neutral Voltage
On	On	Off	Off	Vdc / 2
Off	On	On	Off	0
Off	Off	On	On	-Vdc / 2

2.4.5.2 Flying Capacitor (FC) type MLI (Capacitor Clamping)

The FC type MLI was first established by Meynard et al., in 1992 [52]. Figure 2.2 (a) represents a three-phase, three-level FCMLI. It is considered as a substitute to overcome some of the demerits of NPC type MLI. In this type, capacitors are used for clamping instead of clamping diodes as in the case of NPC type. These capacitors are floating capacitors that connect number of points in the inverter to acquire various output voltage levels. As, in case of three-level NPCMLI, the three-level FCMLI also has the different voltage levels of +Vdc/2, 0, and –Vdc/2. Table 2.2 shows the different switching patterns for the three-level FCMLI and the corresponding output voltage levels.

Similar to the NPCMLI topology, only two control gate signals per phase leg are required in order to eliminate short circuit in the dc-bus capacitor. Though, in the FCMLI the inverted gating signals are related to different power semiconductor switches as compared with NPC. The output voltage levels of the inverter are produced by adding or subtracting the clamping capacitor

voltage with the dc-link voltage. For instance, a zero voltage level is obtained by connecting the output terminal of the inverter to the neutral point '0' through clamping capacitor with opposite polarity with respect to the dc bus voltage. It is also shown in the table that for two switching combinations (ie; S2, S3 ON and S1, S4 ON), the output voltage is zero. This condition of being able to produce the same output voltage level with different switching states is called voltage level redundancy. This redundancy plays a significant role in the capacitor voltage balancing. The capacitor charging state can be controlled by proper selection of the switching states and capacitor combinations. This can reduce the complexity of the capacitor voltage controller for higher voltage levels [53]. Another advantage of this topology is the common dc-bus that reduces the capacitance requirements of the inverter and the capacitors can be pre charged as a group and efficiency of FCMLI is high for fundamental frequency operation.

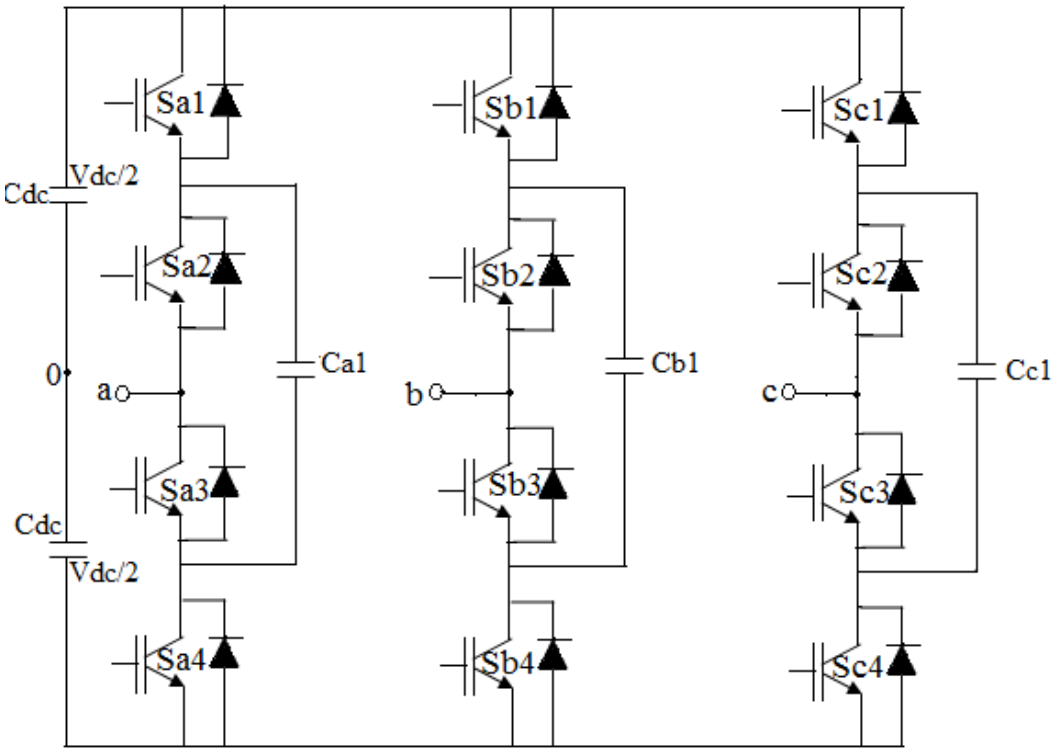


Figure 2.2 Three-level FCMLI

This FCMLI can be stretched to higher number of output voltage levels and can be used as a modular topology by combining a set of semiconductor devices together with one capacitor as a cell. These cells can be connected in cascaded fashion and each one provides one additional voltage level to the output. Yet, the capacitors within each cell of FCMLIs are charged to

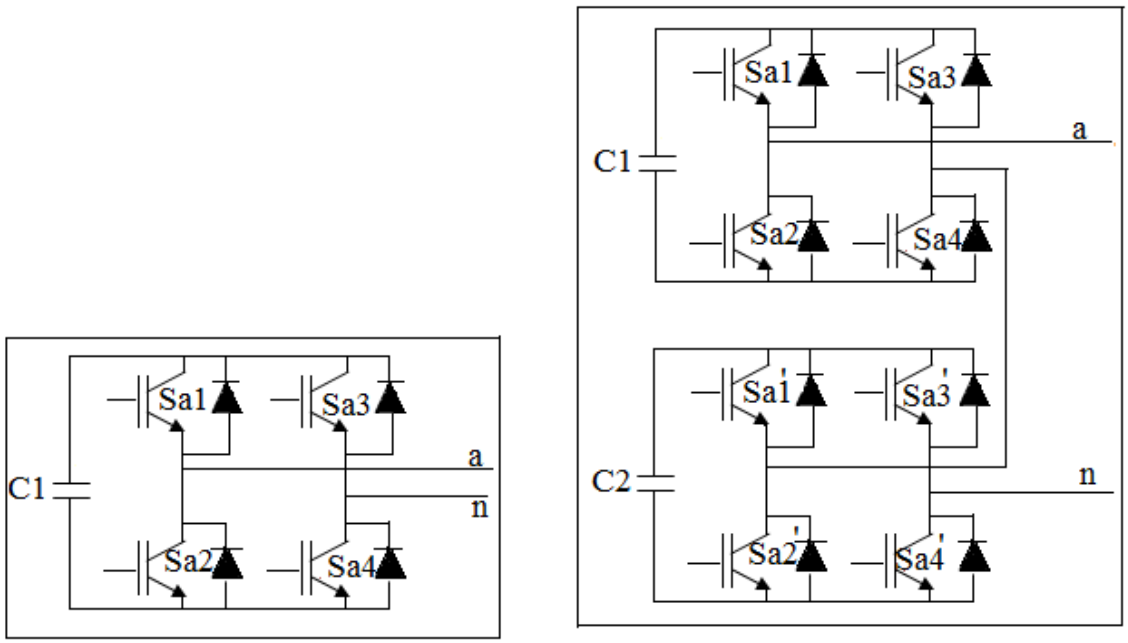
unequal voltages and this is in opposite with the modularity concept. In this topology, as the number of voltage levels increases the number of capacitors also increases. An n-level FCMLI requires a total of (n−1) (n−2)/2 clamping capacitors in each phase in addition to the (n−1) main dc-bus capacitors. The higher number of capacitors and lack of modularity can minimize the reliability of this inverter. For switching frequencies below 1 kHz, the size of the condensers can also become huge because of the fact that the output current flows through clamping capacitor as long as the switching state does not change. Yet, being able to overcome the complexity in the control and hardware, a five-level FCMLI is successfully implemented in STATCOM applications with voltage level up to 6.6 kV [54].

Table 2.2 Possible switching states for three-level FCMLI

S1	S2	S3	S4	Phase-Neutral Voltage
On	On	Off	Off	Vdc / 2
Off	On	On	Off	0
On	Off	Off	On	0
Off	Off	On	On	-Vdc / 2

2.4.5.3. Cascaded H-bridge multilevel inverter (CHBMLI) topology

The cascaded H-bridge multilevel inverters use separate dc sources. This topology can avoid additional clamping diodes or clamping capacitors. Figure 2.3 represents the basic circuit configuration of a single-phase leg of three-level and five-level cascaded H-bridge multilevel inverter (CHBMLI) topology. The output voltage is the addition of the voltage which is produced by individual modules. In a 3-level cascaded inverter, each single-phase, full-bridge inverter produces three different voltages at the output: +Vdc, 0, -Vdc. This is achieved by joining the capacitors serially to the ac side through the switching devices. The resultant output ac voltage magnitude fluctuates from -Vdc to +Vdc with three-levels, and -2Vdc to +2Vdc with five-levels. The staircase waveform is approximately sinusoidal even without any filter. For a three-phase system, the output voltage of the three cascaded inverters is affixed in either star or delta configurations.



(a) (b)

Figure 2.3 Single-phase structures of Cascaded inverter (a) 3-level, (b) 5-level

Cascaded H-Bridge multilevel inverters are capable of attaining the higher number of output voltage levels which is double the number of dc sources. A cascaded multilevel inverter can be built by connecting H-bridge inverter units in cascaded manner that makes modularized layout and stacking. Even though CHBMLIs have good modularity, they use a higher number of switching elements and dc sources [55–57]. Due to the modularity, it is easy to replace one cell or module from the system in case of fault without disturbing the entire system. CHBMLIs can be performed in two configurations; symmetrical and asymmetrical configurations. In the symmetrical mode of operation, each H-bridge is fed with finite dc sources and the value of dc sources is the same for all H-bridges. In this mode, each H-bridge produces similar output voltages and multilevel voltage waveform is produced by cascading these voltages. However, in order to produce a higher number of output voltage levels, a huge number of switching devices and dc sources are needed [58–61]. This can be overcome by asymmetrical configurations where each bridge is supplied with various dc sources and hence each H-bride acquires the potential to produce different output voltages. By combining such voltages, the higher number of voltage levels are obtained in the output voltage [62, 63]. Since it contains a number of cascaded power

conversion modules, the voltage and power levels can be easily scaled. Although the modular structure presents a fairly simple structure, they require a high number of modules to reduce the harmonics and operating frequency. This leads to a more complexity in dc voltage control loop. Though, various existing control strategies can be used to regulate the large number of capacitors voltage [64]. Owing to the lack of a common dc-bus, the output power will be affected by an oscillatory component having the characteristic frequency equal to twice the supply frequency. These fluctuations will be reflected on the dc-bus voltage and therefore each module demands over-sizing of the dc-bus capacitors to provide filtering effect.

2.4.5.5 Comparison of Multilevel inverter topologies for STATCOM applications

The proper selection of the inverter topology for different industrial applications is necessary. The MLI based DSTATCOMs or APFs are widely used in moderate or high voltage electrical network to minimize the voltage stress across switching devices. Introducing multilevel inverters decrease switching losses occurred in the power device and it requires a smaller size filter to mitigate harmonics as compared with two-level inverters. In the last decade, modular multilevel converters (MMC) like cascaded H-Bridge (CHB) topology are widely used for grid-connected applications. This multilevel inverter technique is distinguished as the industry standard for today's power quality compensations and has replaced other conventional inverter topologies, mainly because of its small footprint, highly attainable voltage levels (permitting transformer-less performance), modularity and minimized losses. However, it requires several dc sources. The main objectives of the previous works were to reduce THD, improve switching angle and the switching pattern of the multilevel inverters. Recently, cascaded type capacitive coupled STATCOMs are suggested to minimize the dc-bus voltage requirement [111], and another cascaded type of hybrid topology which consists of various passive elements as filters in cascaded with STATCOMs or APF circuits is proposed to compensate reactive and non-linear loads in distribution systems [112]–[117] and traction power systems [118]–[120]. But these cascaded type techniques have relatively thin reactive power compensation ranges. If the compensating reactive power demand is outside the compensating ranges, their overall performances can significantly deteriorate. To overcome the flaws of different reactive power compensators, another hybrid-STATCOM is presented in [121] that involved a thyristor-

controlled LC (TCLC) section instead of an interface reactor in traditional STATCOM. It requires an additional control strategy to coordinate the TCLC part and the active converter segment to compensate for reactive power. The TCLC part consist of an interfacing reactor, a shunt capacitor, and a thyristor-controlled reactor with low pass filter and has switching angle mistuning issue that makes the design of dc-link voltage difficult. An improved hybrid DSTATCOM technique to mark some practical problems like power rating, filter size, compensation capabilities, and energy loss is presented in [122]. It used an LCL filter circuit at the front end of VSC that provides improved switching harmonics elimination with a very small inductance as compared to the traditional inductor filter. In this technique, a capacitor is connected in cascaded with an LCL filter to lower the dc-bus voltage of the DSTATCOM. It also uses a damping resistor. The LCL filter circuit and damping resistor increase the weight, cost, and size.

The power processing cannot be achieved through any single switch. One method to achieve a high voltage rating is to affix a number of switches in cascaded fashion and operate them simultaneously. However, the cascaded operation of switching devices is troublesome due to tolerances in their characteristics and/or the unavoidable mismatch among the triggering circuits. The major issue is to make sure a uniform voltage sharing among the elements during static and dynamic transient conditions. Furthermore, special arrangements are required to guarantee an uninterruptable working of the device in case of a faulty switch. An easy way to enhance the voltage rating is to utilize modular structure. In these structures, it is possible to increase the total output voltage of the inverter by adding the number of modules that work at low voltage. As mentioned earlier, it is possible to increase the voltage in modular constructions only by raising the number of voltage levels that result in better harmonic performance and reduced power losses. These modular structures also have the ability to balance the capacitor voltages for a high number of voltage levels. So, the modular configurations are often regarded as the best remedy to develop high-power STATCOM, while NPCMLI and FCMLI are more suitable for medium-voltage and low-power applications. Besides this, the structure of separate dc sources is highly suitable for different distributed energy resources such as fuel cell, photovoltaic, and so on. Table 2.3 summarizes different parameters of multilevel inverter topologies conferred in this section.

Table 2.3 Summary of different parameters of MLIs

Parameters / **Type**	**NPCMLI**	**FCMLI**	**CHBMLI**
Switches per phase	2 * (n-1)	2 * (n-1)	2 * (n-1)
Clamping diodes per phase	(n-1) * (n-2)	0	0
Capacitors per phase	(n-1)	(n-1) * (n-2)/2+(n-1)	(n-1) / 2
Loss distribution	Identical with ANPC	Identical	Identical
Maximum practical levels	3-5 levels	5-7 levels	No theoretical limit
Availability	Low	Low	High
Modularity	Not modular	Not modular	Modular
Capacitor size	Small	Large	Large
Low switching	Possible	Possible with large capacitors	Possible with large capacitors
Common dc source	Common	Common	Not common

where 'n' is the number of levels.

2.5 DSTATCOM Control Strategies

The controller plays a significant role in the STATCOM system and presently different control algorithms are demonstrated in the literature. Principally there are two kinds of controller requirement in a STATCOM: (i) Reference current generation technique to produce the reference current from the distorted line current and (ii) Pulse Width Modulation voltage source inverter (PWMVSI) current control technique to produce the triggering pulses to switch the converter.

2.5.1. Reference current generation methods

A number of control strategies have been developed so far. The development of compensation techniques by means of currents or voltages is the significant part of DSTATCOM's control strategy that affects the overall STATCOM performance. The control algorithms can be either time domain or frequency domain [65]. Fast Fourier Transformation (FFT) algorithms, sine multiplication method, and modified Fourier series method are the frequency domain approaches that provide accurate individual and multiple harmonic load current detections and this is suitable for both three-phase and single systems. Since it is based

on the Fourier Transform analysis of the distorted current signals, which involves large mathematical calculations, it results in more complications in the control circuit. Also, non-periodic load currents cause inaccuracies in computation as the Fourier transform is defined for periodic waveforms only. Whereas the concept of algebraic transformations and conventional circuit analysis are utilized in time domain algorithms and are quicker and easy to develop than the frequency-domain approaches. Control strategies in the time domain are based on the instantaneous calculation of compensating signals in the form of current signals from distorted signals. These are mainly utilized for three-phase systems. The main benefit of time- domain approach is its quick response compared to frequency-domain [66]. In [67], the Fryze–Buchholz–Depenbrock power theory was presented. It demonstrates that a nonlinear load that consumes non-sinusoidal currents can be separated into conductance and susceptance at the various harmonics. Once these values are estimated, the harmonics are eliminated via low-pass filter and the required reference currents are derived from the active current components. Artificial Neural Networks (ANNs) [68] were also used to sense harmonics in energy systems by adopting Kalman filters (KF). In [72], a proportional–integral (PI) control technique with lower number of current sensors is proposed to improve terminal voltage profile. The main demerit of PI-based regulation method is the instability as it does not take into account load currents when producing reference signals. The traditional PI and PID controllers are also incorporated to calculate the reference signal by regulating the dc-bus capacitor voltage of the PWM-converter [86]. But, these regulators need a precise linear mathematical derivation of the system that is difficult to achieve under parametric change and distorted load conditions. Chatterjee et al. [73] presented one cycle control technique that is a unified fixed-frequency integration technique for STATCOM. This technique suffers from the demerit of severe current notching with the system feeding non-linear loads.

Hirofumi Akagi suggested three-phase, three-wire shunt active power filter system with an instantaneous reactive power theory and later, this theory is extended to the three-phase system that consists of zero-phase sequence components [5], [11], [12], [18]–[20]. In this, the reference signals are estimated instantaneously by sensing the instantaneous load voltages and currents [17]–[19]. In this method, the control circuit consists of a number of analog multipliers, dividers, and op-amps. This technique is successfully used under various voltage conditions such as distorted, unbalanced and so on. Several other control methods are further developed to control

the DSTATCOM such as dq, pqr [74, 75], Lyapunov based control technique [76] etc. The dq theory is first applied to shunt active power filter by Bhattacharya and is based on the method of calculating the direct and quadrature elements of the currents [7], [8], [16]. The instantaneous power theory is developed by Watanabe et al that is true for steady state as well as transient state, generic voltage and current waveforms [77]. He also presented the traditional active and reactive power theory. The instantaneous power control methods presented in [74, 75], [78-80], are dedicated to converter based structures and their operating characteristics are dependent on the speed of computation and the operating frequency of the digital controllers and the switches. Blaabjerg et. al presented a nonlinear control method for a three-phase, three-wire VSC based shunt compensation. In this, the reference signals are generated from the non-linear load currents by synchronous reference frame strategy [81]. Reyes S piloted an experimental study by considering the original p-q theory, d-q transformation, modified or cross-product formulation, p-q-r reference frame, and vectorial theory. He proved that these approaches are beneficial for the sinusoidal and balanced voltage conditions and if the supply voltage is non-sinusoidal, none of these theories achieve the target in their original development [82]. The synchronous detection (SD) method presented in [69, 70] is based on the calculation of the individual phase voltages. This technique is popular for its improved performance compared to SRF and IRPT for the system under unbalanced load conditions. The original SD algorithm cannot be directly applied to the system without any filters under non-linear loads connected to source inductance because of distorted wave shape of PCC voltage. This condition can be overcome by a simple low-pass filter (LPF) to filter the sensed voltages, but it results the phase shifted waveform from actual signal. A second-order generalized integrator (SOGI) [71] is used to filter the distorted system voltages. It produces two orthogonal signals of base frequency and the outputs of SOGI can be utilized to calculate the magnitude of phase voltages which would avoid the additional peak calculating modules like ‘sample and hold’ circuits. Salem Rahmani [83] developed the nonlinear control method to generate a current signal for a three-phase STATCOM. This strategy offers compensation for reactive, unbalanced, and harmonic load current components. Rondineli [84] proposed an adaptive filter based strategy to enhance the transient response time of harmonic detection technique of STATCOM. A robust adaptive control strategy for STATCOM applications is introduced by Ricardo that perform a multi-task of power-factor (PF) correction, compensation for harmonic current, and non-linear load balancing. The reference signals are

produced by the dc-bus voltage regulator based on the active power balance of the system. By using a PLL circuit, they are aligned to the phase angle of the voltage vector [85]. In the last few years, several artificial intelligence technique based control strategies are developed to generate current reference from the distorted line current [87, 88]. The fuzzy logic system is used to calculate the amplitude of current reference signals and keep the dc-voltage of the PWM-converter fixed. This technique does not require an exact mathematical calculation. It is capable of working in the imprecise inputs and can deal with nonlinearities [89, 90].

2.5.2. PWM-current control technique

In the previous section, the main inverter topologies for DSTATCOM applications have been presented. In order to obtain the desired output voltages, each topology has different switching patterns. A method of generating a switched representation of a waveform is called modulation and is more efficient. Pulse-width modulation control strategies are extensively used to power alternating current circuits with an available dc source or for the conversion of DC to AC. A constant dc input supply is fed to the converter and a controlled AC output voltage is obtained by variable duty cycle. The inverter switching must be controlled to track a reference signal and modulation methods are necessary to determine the triggering control of the converter. Various PWM techniques can be incorporated for the optimization of the switching frequency of each power electronic device and it is the most reliable method to gain a required output voltage waveform. There are two methods to generate a switched waveform; open loop and closed loop. The most popular modulation technique performs well in open loop. It is based on the mean value of the switched waveform to match the mean value of the modulating signal over an interval. The PWM signal with variable duty cycle can be produced using MATLAB-Simulink model or experimental implementation using a digital microcontroller, PWM integrated circuits or simple analog components. The analog PWM control signal needs the production of both modulating and carrier signals that are compared to a comparator that gives output waveform based on the difference between the two input signals. The modulating signal is sinusoidal and it determines the frequency of the output signal and the carrier signal is either a saw tooth or a triangular wave at a frequency higher than the modulating signal. If the carrier wave is at a higher voltage than the modulating, the comparator output is at one state and when the reference signal is at a higher voltage, the output is switched to the next state. In this section, modulation techniques for multilevel inverter are discussed. Like two-level voltage source inverters,

multilevel inverters also use either sine PWM (SPWM) or space vector PWM (SVPWM). SPWM is the most commonly used PWM technique. In SPWM method the high frequency triangular carrier signal is compared to a sine modulating signal which represents the required fundamental frequency component and the relative levels of the two signals are used to regulate the triggering of devices in each phase leg of the inverter [91]. The sinusoidal pulse width modulation (SPWM) techniques are the preferred approach in most applications because of its low harmonic distortion characteristics, fixed switching frequency, and simplicity in implementation.

This SPWM for MLIs can be generated using more than one triangular carrier. For an n-level converter, (n-1) triangular carriers are arranged in adjacent bands across the full linear modulation range of the multilevel converter. The sinusoidal PWM (SPWM) provides fixed switching frequency operation and reduced complexity for MLIs as compared to other modulation techniques. The phase shifted carriers (PSC) and the level shifted carriers (LSC) are the popular sine PWM strategies for multilevel converters [92-94]. The PSC PWM is an extension of two-level sine-triangle PWM of two-level inverters. It is the most common modulation method for flying capacitor type MLI (FCMLI) owing to its modularity [53]. The merits of PSC PWM when applied to FCMLIs are natural balancing of the capacitor voltages. The alternative carrier-based open-loop modulation method for multilevel inverters is the level-shifted PWM (LSPWM) [95]. For ‘m’ number of voltage levels, there is (m-1) carrier waves stacked on adjacent band with respect to each other. Each carrier is shifted identically to generate a continuous band within the full linear modulation range and each of these carriers belonging to particular voltage levels. Previous works [95] [99] [100] have shown that PD-LSPWM achieved the optimum performance for three-phase MLIs in terms of line-line harmonic spectrum. This approach is specifically beneficial for the NPCMLI since each of the carriers belongs to two power switches of the VSI. It also provides the facility for natural balancing of the neutral point voltage for NPC inverter and enhances the harmonic performance of VSI along with the reduction in the calculation time of the digital signal processor [96] [97] [98].

Another popular PWM technique for three-phase VSCs is space-vector pulse width modulation (SVPWM) [13] [14]. The elementary benefit of SVPWM over SPWM is the explicit identification of the pulse placement within each carrier period as an extra degree of freedom,

which has been shown to enhance harmonic performance of the converter. The SVPWM techniques of two-level inverters can also be employed to multilevel inverters [97]. They are able to produce the highest available fundamental output voltage with low harmonic distortion of the output current. David Brod documented an overview of the characteristics and inherent restrictions of PWM current controllers for a poly-phase load.

The hysteresis current controller (HCC) works better except that the inverter operating frequency is higher than required. The switching frequency can be lowered by introducing zero voltage switching [101]. Akira Nabae presented a new feedback control method that is capable of suppressing higher current harmonics in steady state and can solve the sudden current response problems in the transient state [102]. The HCC technique is the most widely employed control technique in DSTATCOM because of its simplicity in implementation and quick dynamic response with capacity to limit the peak current [105]. In this control, current errors are utilized to calculate the next PWM state of the VSI. The current error compensation and pulse generation are carried out in the same control unit simultaneously. The major flaw of this type of controller is the limit cycle oscillations. Bimal K Bose developed an adaptive hysteresis controller for a voltage sourced PWM converter. It keeps the frequency of modulation fixed. This method is applicable to AC drives and other kinds of nonlinear loads [103]. Murat Kale employed this control technique for reactive power compensation and harmonic elimination of three-phase converter. This controller changes the hysteresis bandwidth according to frequency of modulation, supply voltage, dc-link capacitor voltage and slope of the reference compensator current [108]. The problem with this controller is that it ensures more switching power losses owing to high frequency switching that can overcome by adaptive-fuzzy based hysteresis current controller (AFHCC) [109]. AFHCC can be used to estimate the switching signals and to select the optimum value of the decoupling inductance. This technique considers the instantaneous supply voltage and grid current as input variables for defining a systematic hysteresis band to design a look-up and the hysteresis band as an output variable to maintain constant modulation frequency.

Two simple current control strategies are proposed by Marian based on the three-level hysteresis comparators that select appropriate VSI output voltage vectors by switching electrically programmable read-only memory table. The first one operates with current components

represented in a stationary ac components system, and the second one operates with a rotating dc components system. The principle of operation of these two techniques is presented and compared with three independent two- level hysteresis controller in [104]. Dixon suggested different current regulation methods for voltage source converter and validated them practically. He incorporated various controllers such as periodical-sampling controller, triangular-carrier controller and hysteresis current controller for his study. The triangular-carrier controller exhibited best performance in harmonic distortion and has reduced current ripple than other techniques. Yet, this technique with proportional gain introduced issues of overshoot. The periodical-sampling controller performance enhances with moderate time delays and exhibited improved performance when slow power switches are employed. In [106], the author presented a new space-vector-modulation (SVM) based hysteresis current controller. It uses all the merits of the HCC and SVM techniques. This controller estimates a pair of space vectors from a region detector and applies the selected space vector with respect to the main hysteresis controller. A three-level hysteresis current controller for single phase inverter is proposed in [107]. It gains substantial reduction in the amplitude and variation of the operating frequency and enhances efficiency compared to two-level HCC. In recent years, the control techniques based on high level language coding is proposed and developed in DSP / FPGA processor for efficient operation of the filter [110-111].

2.6 Summary

The effects of nonlinear loads and different types of reactive power compensating solutions are reviewed initially. Among the various types of power quality compensation techniques, FACTS devices are found as the most suitable technique to enhance the power quality. For proper compensation in the distribution system, the selection of voltage source inverter plays a very significant role in terms of power loss, efficiency, cost and total harmonic distortion. Various inverter configurations and control schemes suitable for DSTATCOM applications are presented in literatures. Multilevel inverter topologies are capable of producing a higher output voltage levels with the cost of higher number of switching devices.

Increasing number of voltage levels in a multi-level inverter requires an increase in number of semiconductor switches and passive components. The issue of dead time requirement and shoot

through in PWM converters distorts the output waveform and transfers less energy to load. Here is the gap. A three-phase VSI called three-phase Infinite Level Inverter (ILI) is presented to eliminate all the above mentioned issues to a great extent. The device constraint and switching loss at high frequency is substantially minimized owing to reduced input dc voltage. To get same output voltage, the suggested inverter needs only 50 % of the dc-bus voltage compared to sine PWM inverter.

In order to compensate reactive power and harmonic filtering in a better way together with reduced power loss, size, and cost, the research focuses on the modeling and analysis of infinite level inverter (ILI) with reduced dc-link voltage and reduced number of high frequency switches in a DC/AC converter suitable for DSTATCOM applications. It produces an infinite number of voltage levels without any increase in the number of active and passive elements. This ILI topology improves harmonic compensation capability and provides complete reactive power compensation when used as DSTATCOM compared with classical topologies and no LCL filter requirement to achieve this goal. The detailed modeling and working principle of the ILI would be described in the next chapter. The new features of this ILI topology that differentiate it from currently available DSTATCOM inverters discussed above are (i) ILI need not be oversized (ii) reduced dc-bus voltage and (iii) fast response.

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Chapter 3

Modelling and Analysis of VSI based DSTATCOM

3.1. Introduction

Numerous compensation techniques have been introduced in the literature to use either at the distribution or at the transmission lines. DC to AC power electronic converters can be considered as the core of the FACTS devices. The operation and control of these converters are significant especially when medium or high power systems are considered. With the use of PWM converters, the grid side power is not polluted as it is able to control input current magnitude as well as phase angle (lead or lag) to meet with the power quality requirement. Due to the high speed switching converter characteristic, a DSTATCOM contributes a higher response than SVC. To analyze the performance of the DSTATCOM, detailed modeling is essential. This chapter is aimed at the simulation and analysis of a FACTS device known as DSTATCOM or Distribution Static Synchronous Compensator as a remedy to power quality problems. It is a shunt filter which increases the power factor and voltage profile and decreases current harmonic content injected into the source side. It consists of a power electronic voltage-source inverter that acts as either a source or a sink of imaginary power to an electrical system. When joined to a source of power, it can also provide real ac power. This chapter also describes a comparative study of the DSTATCOM employing constant hysteresis band current controller with two different reference current extraction methods namely SRF strategy and IRPT algorithm. The performance of these DSTATCOMs is analyzed theoretically and verified using simulation. The simulation circuit of DSTATCOM is implemented in Matlab/Simulink environment using Simpower systems library.

Principle of operation of DSTATCOM is explained in section 3.2. Section 3.3 briefs mathematical modeling of various control algorithms. Voltage and current controller for VSI based Dstatcom is given in section 3.4. and section 3.5. deals with simulation and simulation results. Finally the summary of the chapter is discussed in 3.6.

3.2 Principle of operation of DSTATCOM

Generally, a DSTATCOM includes a pulse width modulated Voltage Source Converter using SCRs, MOFETs or IGBTs, a dc-bus capacitor and a coupling reactor which connects the inverter output to the distribution lines. The capacitor is connected to the inverter as input. The VSI is joined in parallel to the network at the point of connection (PoC) as shown in figure.3.1. The load current composed of three elements – real, imaginary and harmonic. The notion is to control the converter in such a way as to make it provide the harmonic and reactive current demands of the load so that the grid needs to provide the real current component only. Consequently, the source current becomes pure sine wave and in-phase with the grid voltage on connecting the DSTATCOM. Ideally, it is viable to provide the harmonic and reactive current demand of the load with a voltage source inverter (VSI) having a dc bus condenser and without any exterior power supply as the net power supplied by the DSTATCOM during any given fundamental period is zero. However, practically a little amount of real power is drawn from the source to compensate for the power losses in the system. This is the basic operating principle of a DSTATCOM.

From the brief description given above, it is clear that the design of a DSTATCOM has two major parts:

1. Generation of current reference that consists of calculating the harmonic and reactive currents absorbed by the load.
2. Controller design (It is the controller which makes the DSTATCOM current to track the reference).

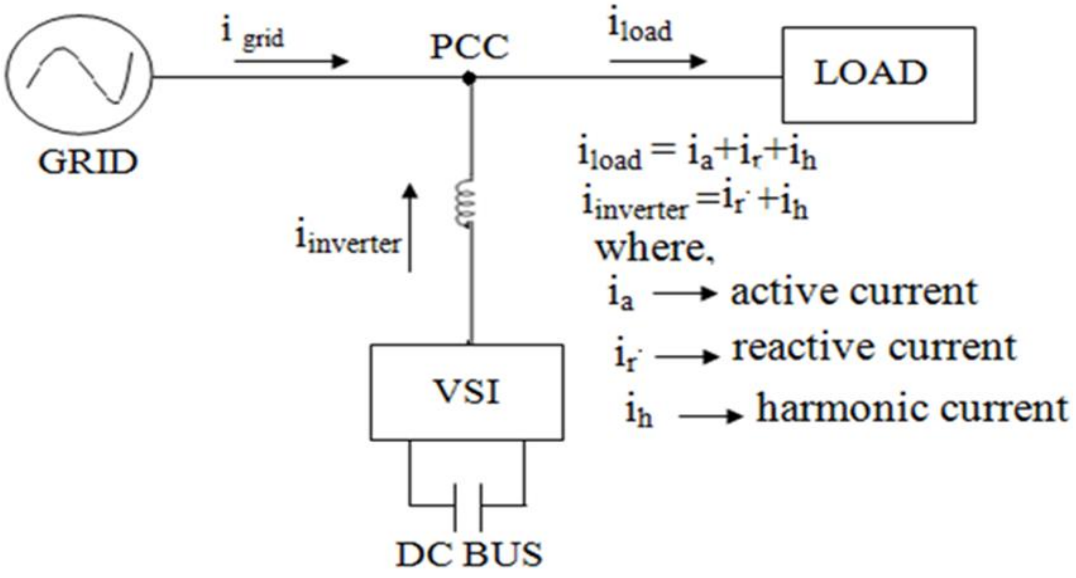


Figure 3.1 Voltage source inverter based DSTATCOM

Most of the control strategies reported in the literature have been restricted to simulation analyses**.** The instantaneous reactive power theory (IRPT) [11] and the synchronous reference frame (SRF) technique are the extensively used control strategies as per literature [12], [13] for a grid connected application. In a three-phase system, reactive power can be conveniently regulated with the use of SRF and IRPT methods with two orthogonal axes [13].

3.3 Mathematical modeling of various control algorithms

3.3.1 Synchronous Reference Frame (SRF) Strategy

The synchronously rotating reference frame method uses co-ordinate transformations to extract the current reference by employing popular Clarke's and Park's transformations. These transformations minimize the calculations involved in the current reference generation. Once the controller output is attained, reverse transformations are used to transform the rotating reference frame variables back into the actual three-phase quantities.

3.3.1.1 The Clarke's Transformation

Consider a three-phase balanced system given by equations (3.1 to 3.3) as follows,

$V_R = V_m \sin(\omega t - \phi)$.....(3.1)
$V_Y = V_m \sin(\omega t - \phi - 120)$.....(3.2)
$V_B = V_m \sin(\omega t - \phi - 240)$.....(3.3)

For a balanced system, just two variables can define the entire system rather than three parameters. Knowing any two parameters of (V_R, V_Y, V_B), the third equation can be expressed from the equation $(V_a + V_b + V_c = 0)$ and any non-sinusoidal balanced three-phase network can be demonstrated by just two variables. This concept led to the popularity of the transformation of a three- phase balanced system in (a, b, c) plane to a two-axis plane (α, β) by using Clarke's transformation.

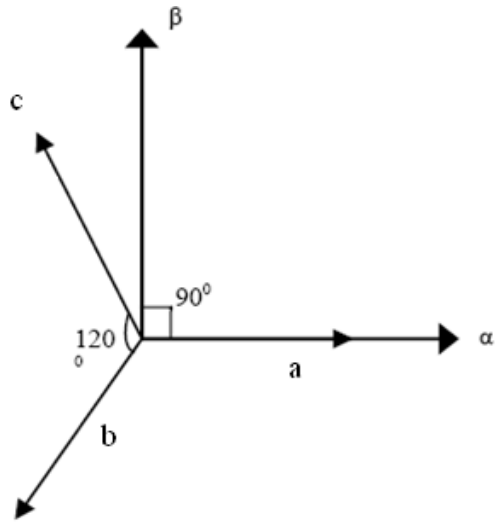


Figure 3.2 a-b-c to α-β frame transformation

To write the equations of transformation, the vectors 'b' and 'c' need to undergo an orthogonal decomposition along 'α' and 'β' axis. From figure 3.2, it can be written

$\alpha = a - \frac{1}{2}b - \frac{1}{2}c$.....(3.4)

$\beta = \frac{\sqrt{3}}{2}b - \frac{\sqrt{3}}{2}c$.....(3.5)

In compact matrix form, the above equations appear as,

$$\begin{bmatrix}\alpha\\ \beta\end{bmatrix}=\begin{bmatrix}1 & -\frac{1}{2} & -\frac{1}{2}\\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2}\end{bmatrix}\begin{bmatrix}a\\ b\\ c\end{bmatrix}\text{.....(3.6)}$$

The reverse transformation of the above equation is;

$$\begin{bmatrix}a\\ b\\ c\end{bmatrix}=\frac{2}{3}\begin{bmatrix}1 & 0\\ -\frac{1}{2} & \frac{\sqrt{3}}{2}\\ -\frac{1}{2} & -\frac{\sqrt{3}}{2}\end{bmatrix}\begin{bmatrix}\alpha\\ \beta\end{bmatrix}\text{.....(3.7)}$$

The system of transformation equations (3.6) and (3.7) constitute Clarke's transformation. This transformation allows to manage with just two mathematical equations instead of three equations. Thus, it saves a lot of computational effort and time. The three-phase balanced system of grid voltage equations 3.1 to 3.3 appear in the stationary α-β plane using equation (3.6), as given below;

$$v_\alpha = \frac{3}{2}V_m \sin(\omega t)\text{.....(3.8)}$$

$$v_\beta = -\frac{3}{2}V_m \cos(\omega t)\text{.....(3.9)}$$

Now, we define $\bar{V} = V_\alpha + jV_\beta$ where 'j' is the imaginary operator. '$\bar{V}$' is called space vector. Applying the definition of space vector to equations (3.8) and (3.9)

$$\bar{V} = V_\alpha + jV_\beta$$

$$\bar{V} = \frac{3}{2}V_m \sin(\omega t) - j\frac{3}{2}V_m \cos(\omega t)$$

$$\bar{V} = -j\left(\frac{3}{2}V_m \cos(\omega t) + j\frac{3}{2}V_m \sin(\omega t)\right)$$

$$\bar{V} = -j\frac{3}{2}V_m e^{j(\omega t)}$$

$$\bar{V} = \frac{3}{2}V_m e^{j(\omega t-90)}\text{.....(3.10)}$$

The usefulness of the space vector $\overline{V}$ is that it gives a good insight into how the three-phase quantities appear in the α-β plane.

The following facts can be concluded from the equation (3.10);

1. The amplitude of the space vector is a fixed and equal to 1.5 times the amplitude V_m of the three-phase sinusoid.
2. When plotted with the (α-β) axes as (x-y) axes, the space vector starts at -90° and rotates in the anti-clockwise direction.
3. The space vector completes 'f' revolutions per second where 'f' is the three-phase system frequency in 'Hz'.
4. At the time 't' from the reference time (t = 0), the space vector would have moved away from -90° by 'ωt' radians in the anti-clockwise direction. Figure.3.3 depicts the above facts pictorially.

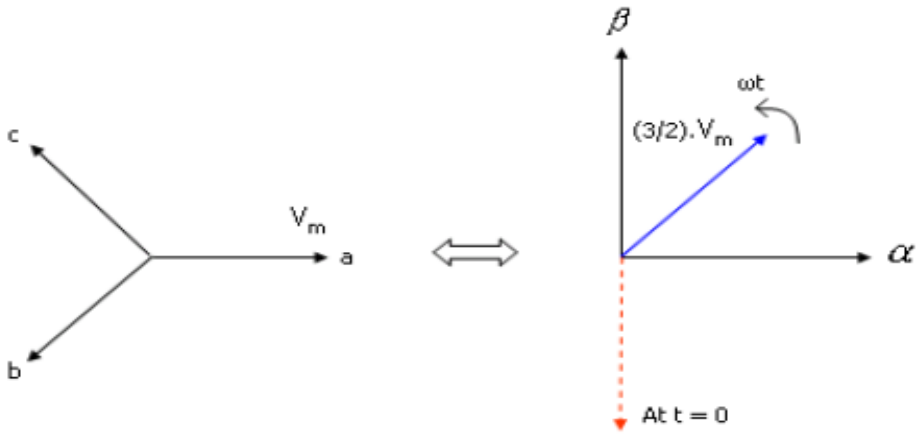


Figure 3.3 Three phase balanced voltages as space vector in α-β plane

3.3.1.2 Reactive current reference generation

Let's assume that the set of balanced three phase line currents that flow from the grid to be,

$$i_a = I_m \sin(\omega t - \phi) \quad \text{.....(3.11)}$$
$$i_b = I_m \sin(\omega t - \phi - 120) \quad \text{.....(3.12)}$$
$$i_c = I_m \sin(\omega t - \phi + 120) \quad \text{.....(3.13)}$$

Then, the grid voltage and line current space vectors will appear in the α-β axis as shown in figure 3.4. Now, as shown in figure.3.5, the current space vector can be split into two component

vectors; one is in phase with the (grid) voltage space vector and the other is lagging the voltage space vector by 90^{o}.

From the earlier discussion, the following facts can be deduced:

1. The in-phase component corresponds to a three-phase system of currents that are in-phase with the three-phase grid voltages and represents the real component of the load current.
2. The lagging component corresponds to a three-phase system of currents which lag the corresponding three-phase grid voltages by 90^{o} and represents the reactive element of the load current. Further, from the sign of the lagging component, it can be said that whether the load is inductive or capacitive. A positive sign indicates an inductive load whereas a negative sign represents a capacitive load.

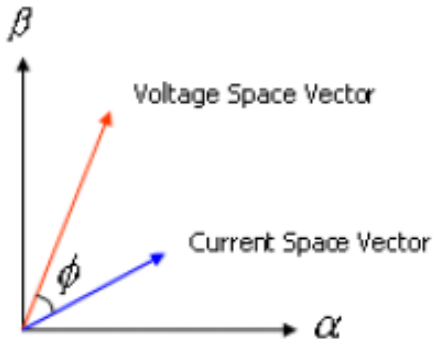


Figure 3.4 Grid voltage and line current space vectors

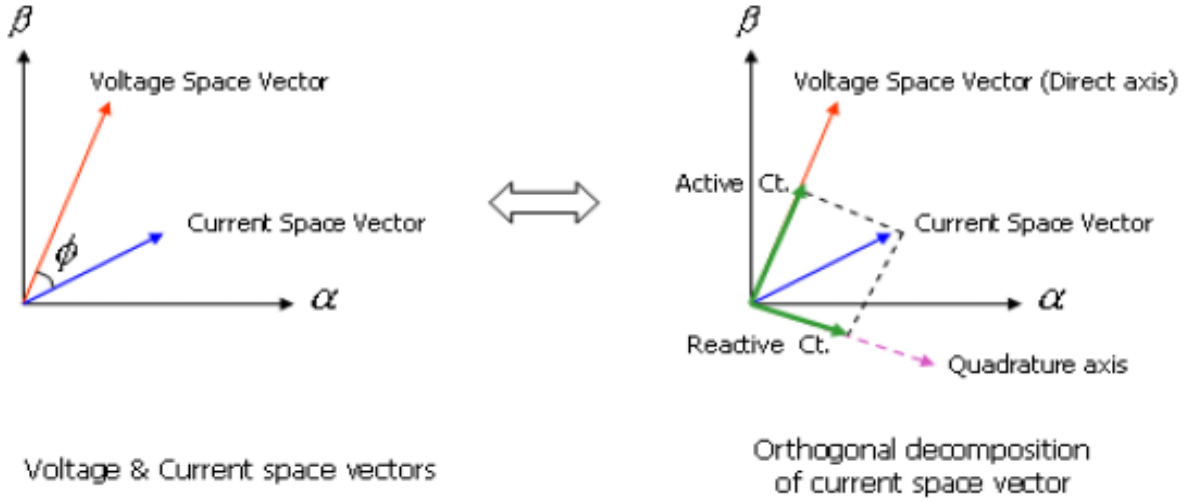


Figure 3.5 Decomposition of current space vector into its component vectors

Thus, the current reference for reactive current compensation can be obtained in the α-β plane by the following two simple steps:

1. Track the angle between the voltage and current space vectors continuously.

Let the angle be 'ϕ',i.e. $\phi = \angle\bar{V} - \angle\bar{I}$,

2. Then,

   a. Instantaneous real component of current = $|\bar{I}|\cos\phi$ and

   b. Instantaneous imaginary current component = $|\bar{I}|\sin\phi$

3.3.1.3 The Park's transformation

Park's transformation is nothing but finding the different components of the load current along the direction of the voltage space vector and at quadrature to it as shown earlier in figure 3.4. The voltage space vector is taken as the direct axis and an axis leading the direct axis by 90^{o} is taken as the q-axis as shown in figure 3.6.

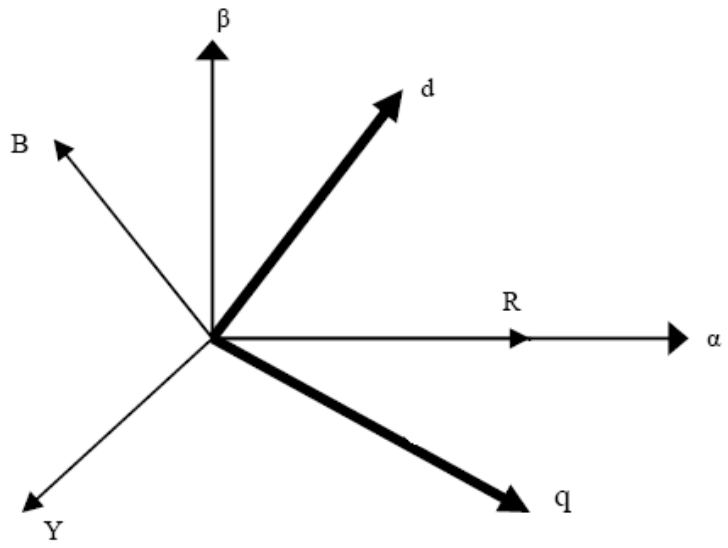


Figure 3.6 α-β to d-q transformation

The benefit of considering the voltage space vector in one of the axes in the direct and quadrature frame is that the d-axis element and q-axis element of fundamental current would directly give the real and imaginary parts respectively (However, the q-component will be negative for an inductive load and positive for a capacitive load). Since the d-axis is always aligned along with the voltage space vector and the voltage space vector is rotating 'f' times every second in the clockwise direction, the transformation actually affects a conversion to a rotating frame of reference. The equations of transformation can be arrived at easily by decomposition of α and β components along the d and q axis. Figure 3.7 shows the decomposition of one of the components (α-component) along the d and q axis.

From figure 3.7,

$$d = \alpha \cos\theta + \beta \sin\theta \quad \text{.....(3.14)}$$

$$q = -\alpha \sin\theta + \beta \cos\theta \quad \text{.....(3.15)}$$

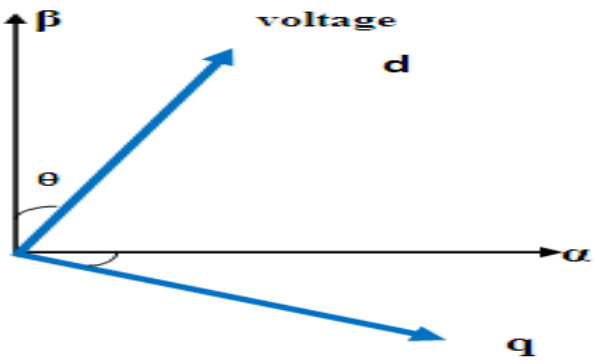


Figure 3.6 d-q plane defined

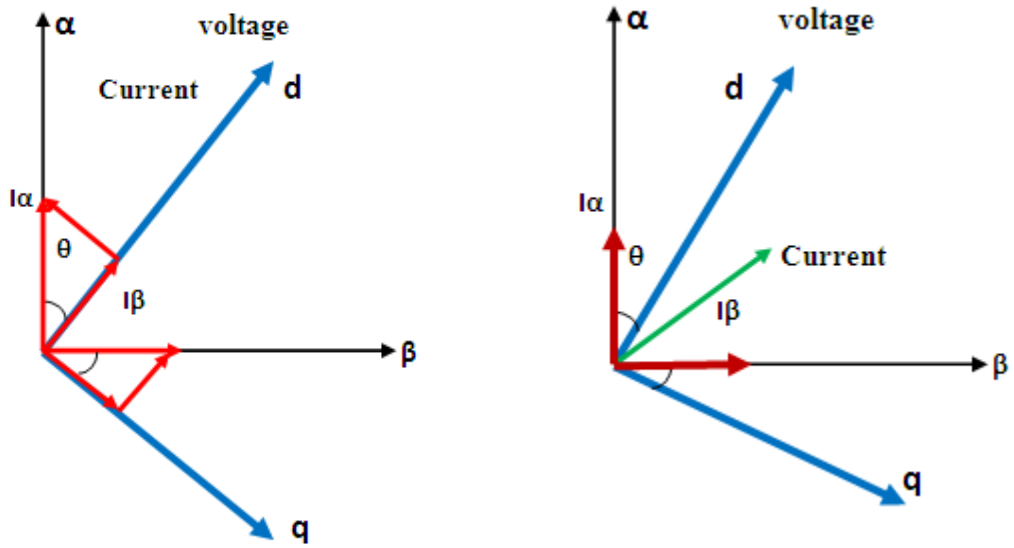


Figure 3.7 Park's Transformation

The above equations can be written in the matrix form as given below;

$$\begin{bmatrix} d \\ q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} \alpha \\ \beta \end{bmatrix} \quad \text{.....(3.16)}$$

The reverse transformation is given by the matrix equation,

$$\begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} d \\ q \end{bmatrix} \quad \text{.....(3.17)}$$

The system of transformation equations (3.16) and (3.17) constitute the Park's transformation. Here the transformation matrix consists of variables rather than constants. This is because these are shifting to a plane which is rotating continuously. In order to do the transformation, it requires cos θ and sin θ that are usually referred to as cos and sin unit vectors respectively. Figure 3.8 explains about finding cos and sin unit vectors.

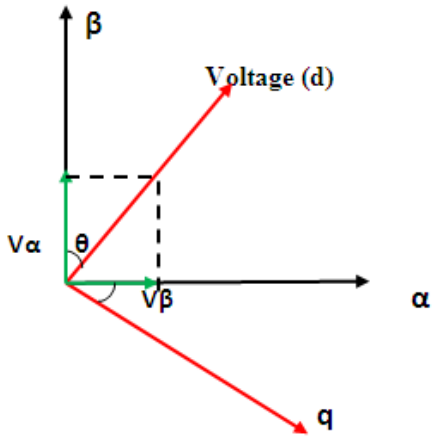


Figure 3.8 Unit vectors

From figure 3.8,

$$\cos\theta = \frac{|V_\alpha|}{|V|} = \frac{\frac{3}{2}V_m \sin(\omega t)}{\frac{3}{2}V_m} = \sin(\omega t) \quad \text{.....(3.18)}$$

$$\sin\theta = \frac{|V_\beta|}{|V|} = \frac{-\frac{3}{2}V_m \cos(\omega t)}{\frac{3}{2}V_m} = -\cos(\omega t) \quad \text{.....(3.19)}$$

From the above equation, it is evident that the unit vectors can be produced by changing the grid voltage to α-β frame and then dividing the α-component and β-component by the space vector amplitude $\left[\sqrt{|V_\alpha|^2 + |V_\beta|^2}\right]$.

The angular displacement θ must be continuous, but the angular velocity associated with the change of variables is unspecified. The frame of reference may rotate at any constant, varying angular velocity, or it may remain stationary. The angular velocity of the transformation can be chosen arbitrarily to best fit the system equation solution or to satisfy the system constraints. The change of variables may be applied to variables of any waveform and time sequence; however, the transformation given above is particularly appropriate for an a-b-c sequence. Park's Transform is usually split into CLARKE transform and one rotation. Clarke converts balanced three phase quantities into balanced two phase orthogonal quantities.

3.3.1.4 Extraction of current reference in the d-q frame

In a balanced three-phase loads that absorb real, imaginary and harmonic currents, the total current is represented as a sum of sinusoids of fundamental and harmonic frequencies. For generating the reference current for compensation, it is necessary to know how these different components appear in the d-q plane. To understand this, consider a balanced three-phase system with a grid frequency of ω_v (represents the fundamental frequency) and a load current component of arbitrary frequency ω_i (The component might be the fundamental or any of the harmonic frequencies) as shown below:

Grid Voltage Load Current

$$v_a = V_m \sin(\omega_v t) \qquad i_a = I_m \sin(\omega_i t - \phi)$$
$$v_b = V_m \sin(\omega_v t - 120) \qquad i_b = I_m \sin(\omega_i t - 120 - \phi)$$
$$v_c = V_m \sin(\omega_v t + 120) \qquad i_c = I_m \sin(\omega_i t + 120 - \phi)$$

From the earlier discussion of unit vector generation,

$$\cos\theta = \sin(\omega_v t)$$
$$\sin\theta = -\cos(\omega_v t)$$

Now, the transformation of the currents to the d-q plane is as follows,

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \sin\omega_v t & -\cos\omega_v t \\ \cos\omega_v t & \sin\omega_v t \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}$$

$$\Rightarrow \begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \sin\omega_v t & -\cos\omega_v t \\ \cos\omega_v t & \sin\omega_v t \end{bmatrix} \begin{bmatrix} \frac{3}{2} I_m \sin(\omega_i t - \phi) \\ -\frac{3}{2} I_m s \cos(\omega_i t - \phi) \end{bmatrix}$$

$$\Rightarrow \begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \frac{3}{2} I_m \cos[(\omega_i - \omega_v)t - \phi] \\ \frac{3}{2} I_m \sin[(\omega_i - \omega_v)t - \phi] \end{bmatrix} \text{.....(3.20)}$$

From the equation (3.20), it can be concluded that;

1. When $\omega_i = \omega_v$, i.e. for fundamental component of current,

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \frac{3}{2} I_m \cos(-\phi) \\ \frac{3}{2} I_m \sin(-\phi) \end{bmatrix}$$

From the expression, it is evident that the fundamental component appears as dc in the d-q plane. Further, when $\varphi = 0^o$, only i_d is non-zero as expected since $\varphi = 0^o$ represents a purely active fundamental current and it should be overlap with the voltage space vector or equivalently the direct axis. Similarly, for $\varphi = \pm 90^o$, only i_q is non-zero representing that reactive fundamental current appears only along the q-axis.

2. When $\omega_i \neq \omega_v$ i.e. for harmonic load currents, both d and q axis currents are non-zero, of equal amplitude and both are sinusoidally varying. This implies that the harmonics appear as ripples in the d and q axes. From the above observations, it can have the following rules for current reference extraction in the d-q plane,

    1. To compensate for reactive current, the dc element in the quadrature axis is served as the reference.

    2. For harmonic current elimination, the ac element in the d and q axes is taken as the pre set value.

    Thusly for both reactive and harmonic compensation, a high pass filtered (that blocks only the dc component) direct axis element and the whole q-axis element is considered as the reference current. Here, the high pass filter for the direct axis is realized via a low pass filter.

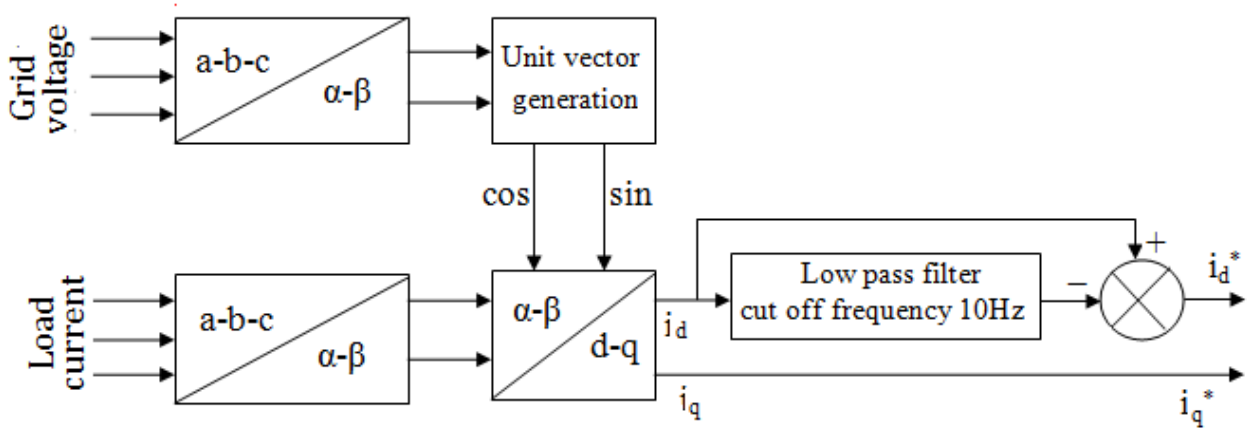


Figure 3.9 Reference current extraction method for the compensation

The block diagram representation for composite compensation of both reactive and harmonic currents is shown in figure 3.9.

3.3.1.5 Phase-Locked Loop (PLL)

A PLL circuit is utilized to synchronize the reference current with the source. It converts the three-phase voltages into the direct and quadrature axes, uses the filtered source voltage and produces improved results. A phase-locked loop (PLL) algorithm is utilized to calculate the main grid phase angle, allowing the production of sin (Φ) and cos (Φ) that define the synchronous unit vector for the SRF strategy. The ac quantities of the system are projected on a d-q plane that is rotating at angular speed. In steady state, the ac quantities are sinusoidal functions of the grid frequency. If the d-q plane angular speed is adjusted to the grid frequency, the transformed quantities become time-invariant in steady-state that simplifies the controller design. This is achieved by means of a PLL.

3.3.2 Instantaneous Reactive Power Theory (IRPT)

This theory involves the transformations of voltages and currents from the three-phase quantities to α-β orthogonal coordinates, and calculation of instantaneous power on these variables. So this principle always considers the three-phase network as a unit system; not a superposition or sum of three single-phase systems. It works in a steady state or transient state as well as for generic voltage and current waveforms that are highly suitable for real-time control. The three-phase quantities (abc) are constant on the same plane and with a phase shift of 120^0. The instantaneous space vectors, voltage v_a and current i_a set on a -axis, v_b and i_b on b -axis, and

v_c and i_c on c -axis. In p–q theory, three-phase instantaneous space vector voltages/currents are converted into two-phase α-β frame by Clarke's transformation as follows.

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \text{.....(3.21)}$$

and

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \text{.....(3.22)}$$

The instantaneous apparent powers in α-β frame are defined as a product of voltage vector *v* and complex conjugate of current vector *i**;

$$S = vi^*$$

$$= (v_\alpha + jv_\beta)(i_\alpha - ji_\beta)$$

$$= (v_\alpha i_\alpha + v_\beta i_\beta) - j(v_\alpha i_\beta - v_\beta i_\alpha)$$

This is of the form $p - jq$, where

$$p = V_\alpha I_\alpha + V_\beta I_\beta$$
$$q = V_\alpha I_\beta - V_\beta I_\alpha$$

where 'p' is the instantaneous active power and 'q' is the instantaneous reactive power. In matrix form

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \text{.....(3.23)}$$

The 'p' and 'q' values can be represented in terms of oscillatory and average components. In a balanced sinusoidal grid voltage conditions, the dc power elements are related to the first harmonic current of positive sequence, and the oscillatory terms demonstrate all higher order

current harmonics including the first order harmonic current of a negative sequence. Generally, for the realization of defined instantaneous real and imaginary power transfer, current components should be determined as:

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} p \\ q \end{bmatrix} \text{.....(3.24)}$$

The reference compensation currents in α-β frame is given by

$$\begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix}^{-1} \begin{bmatrix} p^* \\ q^* \end{bmatrix} \text{.....(3.25)}$$

where p^* and q^* are the real and imaginary powers that are to be compensated and harmonic active and reactive powers extraction are accomplished using low-pass and high-pass filters respectively. The instantaneous values of the three-phase compensating currents are determined by inverse transformation technique from α-β frame to a-b-c frame.

$$\begin{bmatrix} i_a^* \\ i_b^* \\ i_c^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} \text{.....(3.26)}$$

This theory has some interesting features like simplicity in implementation and excellent dynamic response. Yet, under unbalanced voltage conditions, it results in very high current distortion.

3.4 Voltage and current controller

A voltage regulator (Proportional Integral (PI) controller) is utilized to generate the current reference proportional to the input power required to keep the constant dc-link voltage. This reference current is multiplied by a sinusoidal unit vector derived from the PLL and thus the reference currents for each phase are produced. Figure 3.10 shows the block diagram representation of the control circuit of PWM converter.

In order, the source current to follow the reference current, proper switching pulses have to be generated. For these purposes, several PWM methods like sinusoidal PWM (SPWM), space vector PWM (SVPWM), Hysteresis controllers, or one cycle control technique may be used. Among these, hysteresis current controllers are simple to implement as it employs comparators to trigger between the specified hysteresis bandwidth. It offers excellent dynamic performance as it acts quickly [66]-[67]. In a conventional hysteresis controller, the comparators switch between the fixed bandwidths. The bandwidth is constant irrespective of the dynamic nature of current. The hysteresis bandwidth (HB) together with the current dynamics decides the switching instants and hence the switching frequency. This technique is very simple, provides a fast dynamic response, decreases steady-state error, minimum hardware and software requirement for implementation, and no need for information on system variables.

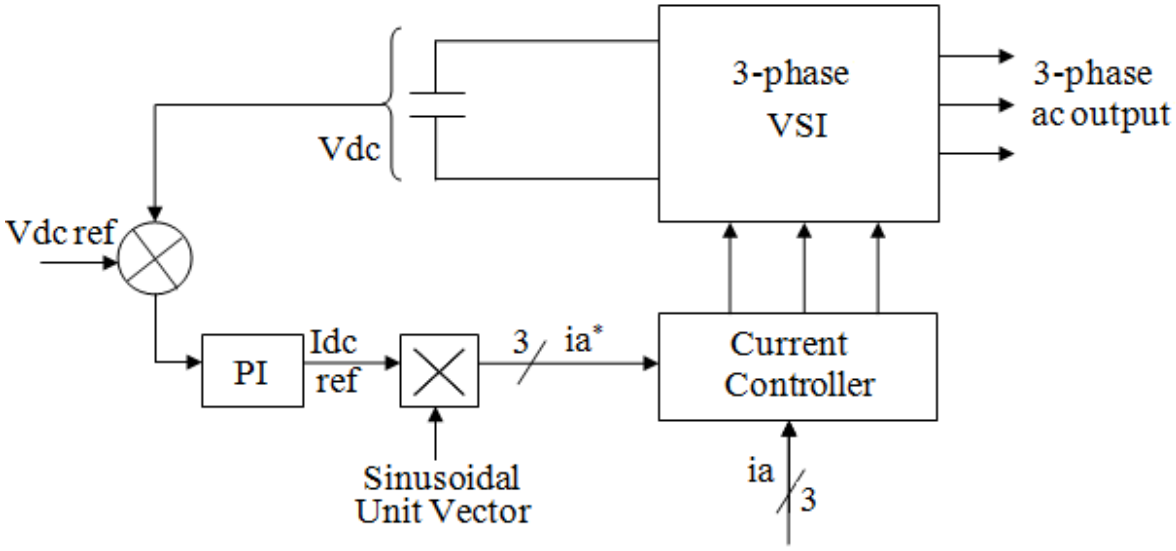


Figure 3.10 Control circuit of PWM inverter

The circuit configuration of a 3-phase hysteresis controller is given in figure 3.11. Actual currents are subtracted from respective reference currents and are given to the hysteresis controller having a band of 2 HB (-HB to +HB). If the difference of actual current and reference current is higher than or equal to +HB, the top switch is turned ON and bottom switch is turned OFF, which causes an increase in the actual current towards the upper limit of hysteresis band . When the difference of actual current and reference current becomes less than or equal to -HB, the top switch in a leg is turned OFF and the bottom switch is turned ON. The actual current is

therefore expected to reduce. In this, I_a, I_b and I_c represent the actual currents in phase 'a', phase 'b' and phase 'c' respectively and I_a (ref), I_b (ref) and I_c (ref) stand for the respective reference currents. Signals (a_p, a_n), (b_p, b_n) and (c_p, c_n) correspond to the output signals to the switches of phases 'a', 'b' and 'c' respectively. Signals a_p and a_n are the switching pulses to top and bottom switches of phase 'a' respectively. The symbol HB represents hysteresis band. As an example if $I_a - I_a$ (ref) $\leq$ +HB, $a_p = 1$ and $a_n = 0$ and if $I_a - I_a$ (ref) $\geq$ - HB, $a_p = 0$ and $a_n = 1$.

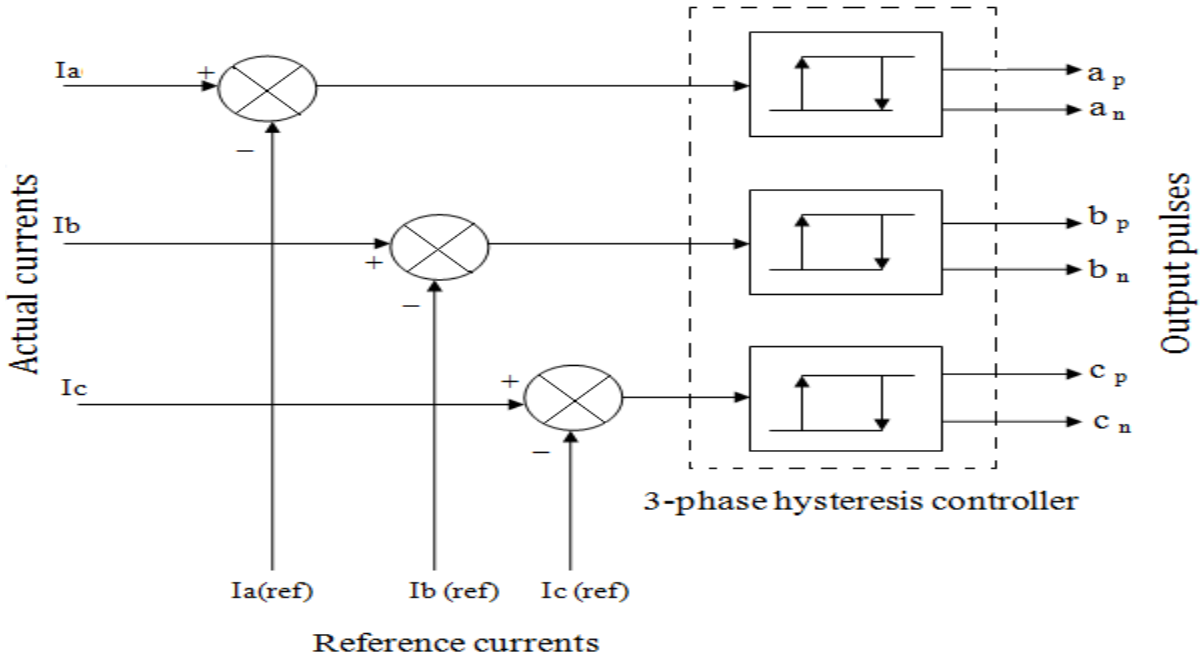


Figure 3.11 Schematic diagram of a hysteresis controller

The conceptual representation of the complete DSTATCOM model is shown in figure 3.12. The current references generated from the load currents according to the selected algorithm are given as the reference signals to the inner current regulator. This controller has the task of generating an output signal similar to its reference.

The basic converter topology of three-phase, three wire voltage source converter is shown in figure 3.13. This basic topology consists of six power transistor switches with anti parallel diodes. The dc voltage source can be either a battery bank or solar photovoltaic cells. The voltage source is assumed to be stiff. Inverter designs normally use pulse width modulation (PWM) to produce a sine wave from the DC voltage

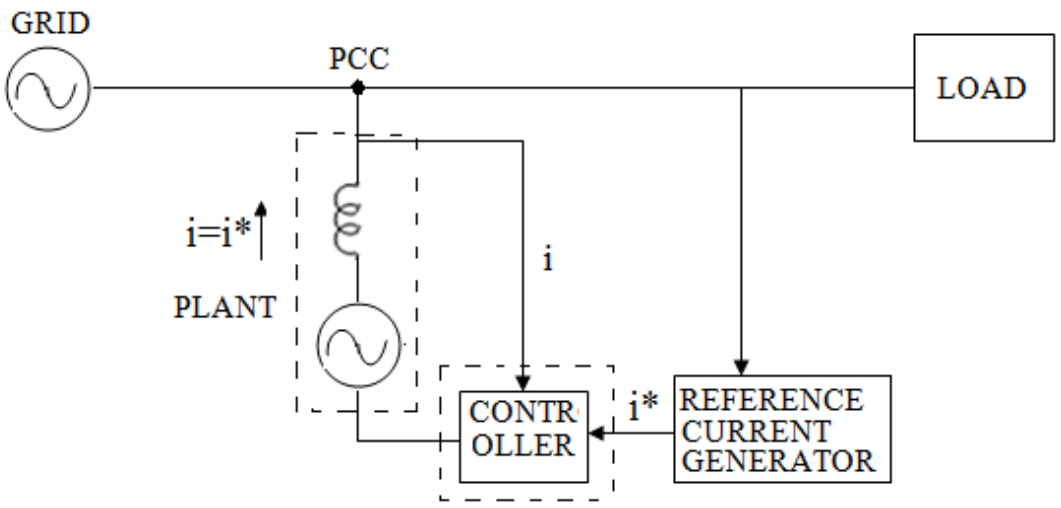


Figure 3.12 Conceptual demonstration of the complete system (DSTATCOM)

The line to line RMS voltage of SPWM VSI is given by the equation;

$V_{LL} = 0.612\ m\ V_{dc}$

Where V_{LL} is the output AC voltage

m is the modulation index, and

V_{dc} is the input DC voltage

From the above equation, it is clear that to produce a three-phase RMS voltage of 415 V, the dc-bus voltage of 678 volts is required for a given values of modulation index (m = 1).

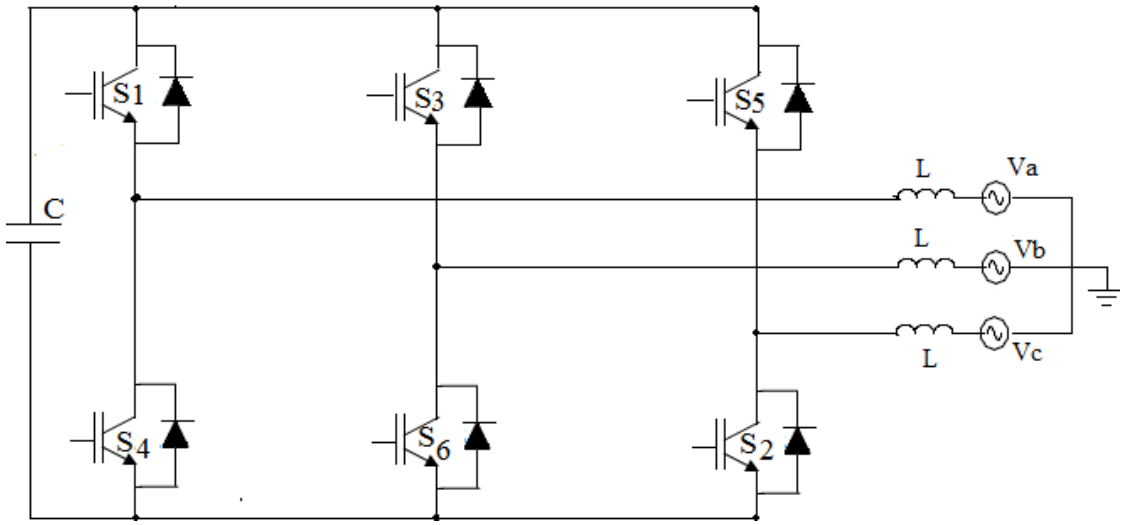


Figure 3.13 Circuit diagram of three-phase voltage source converter topology.

3.5. Simulation and Simulation Results

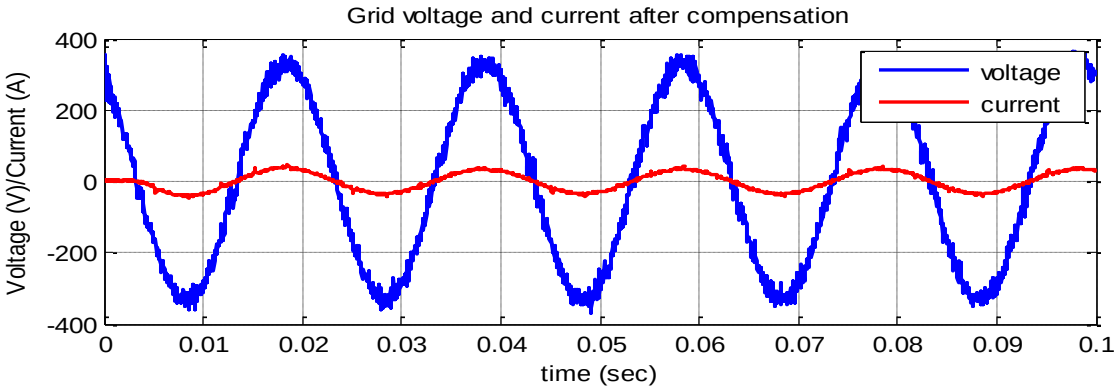
The DSTATCOM circuit model is developed in Matlab/Simulink environment. A fixed non-linear load that consists of a three-phase diode bridge rectifier in parallel with RL load is always connected to the network to analyze the performance of the DSTATCOM. A two-level VSI (figure 3.13) based DSTATCOM is connected at the load side to provide compensation. Here, the main goal of the DSTATCOM is to provide reactive power compensation and harmonic filtering. The PWM-voltage sourced inverter with a dc-bus capacitor is affixed to the point of connection (PoC) through interfacing reactor (figure 3.1). The coupling reactor suppresses the higher order harmonic components caused by the switching operation of the power semiconductor switching devices. Reduction of current harmonics is attained by injecting equal but opposite current harmonic components with the PoC, thereby neglecting the original distortion and enhancing the quality of power in the distribution network.

Table 3.1 Simulation parameters

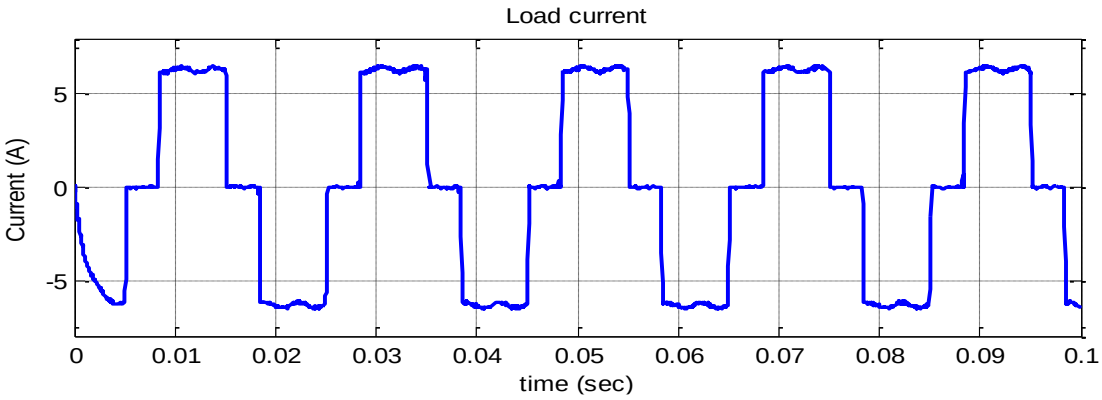
Parameters	**Value**
Grid Voltage and frequency	415 V, 50 Hz
Coupling Reactor	10 mH
DC-link Capacitor	2000μF
DC-link Voltage	680 V
Proportional gain (Kp)	0.4
Integral gain (Ki)	20
Active power	2500 W
Inductive Reactive power	1000 var

Simulation of the DSTATCOM is carried out with two different reference current extraction algorithms such as IRPT and SRF strategy. Source voltage and load currents are used to generate sin-cos unit vector and current references (figure 3.9). PI controller with the proportional and integral gains of 0.4 and 20 respectively is used to control the dc-link voltage to a fixed value. The constant band hysteresis current regulator with fixed band of 0.5 is used to produce

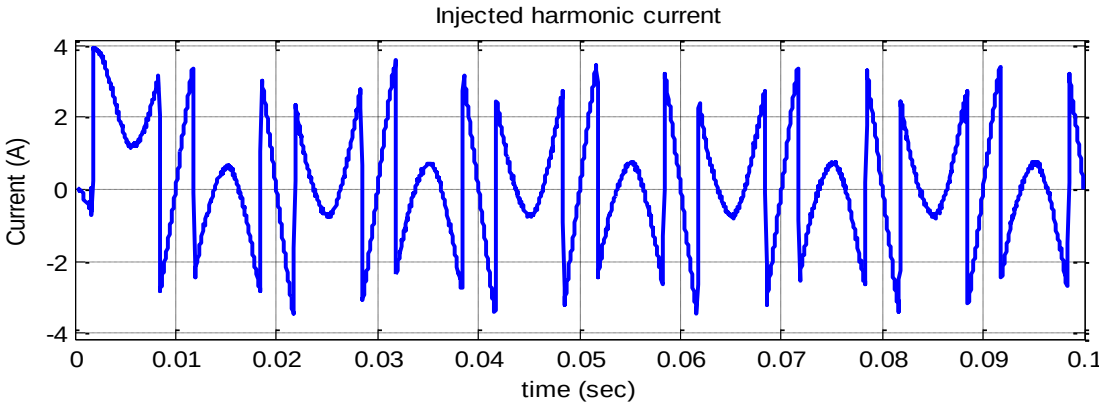
switching pulses for the converter operation. The simulation variables used for the simulation are given in table 3.1. Simulation results using IRPT algorithm are demonstrated in figure 3.14. From the figure 3.14 (a), the source voltage and current after compensation are in-phase and the dc-bus voltage requirement for the compensation is 680 volts.



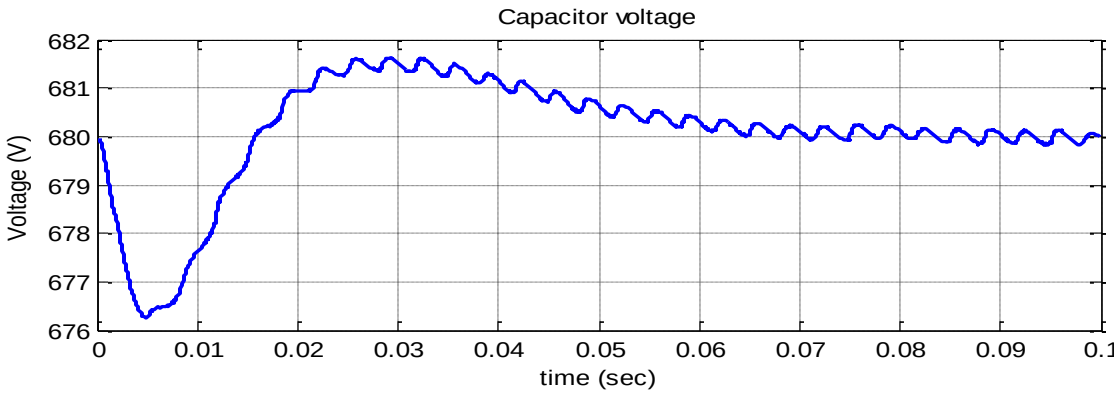
(a) Grid voltage and current



(b) Load current



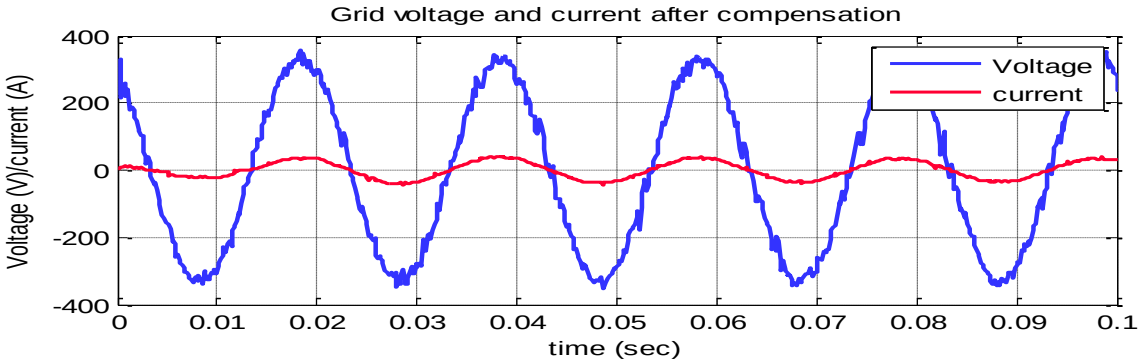
(c) injected harmonic current



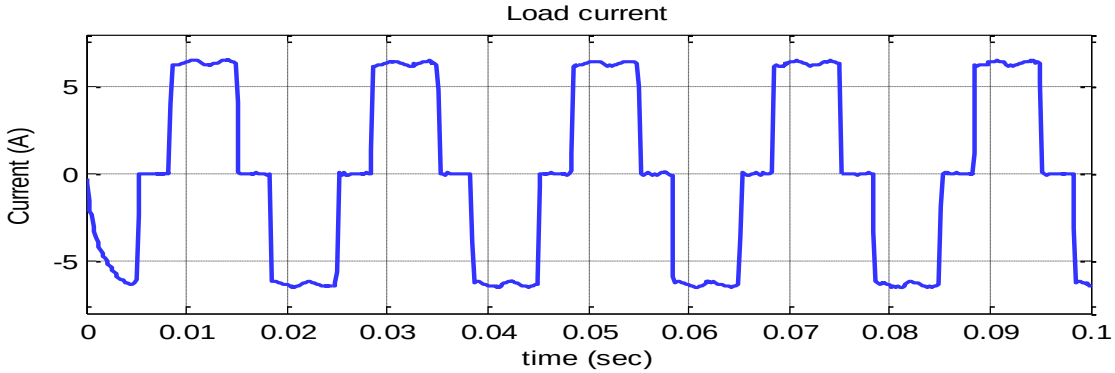
(d) dc-link voltage

Figure 3.14 Simulation results using IRPT algorithm

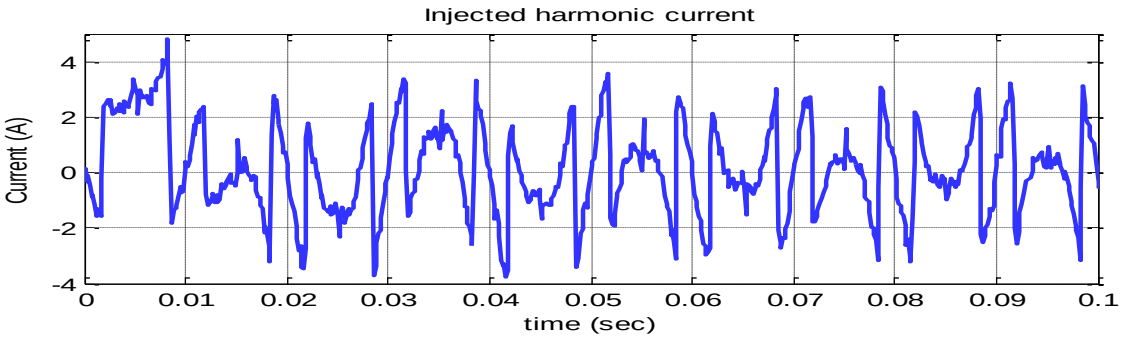
In figure 3.15, simulation results of the DSTATCOM using SRF strategy are shown. In this figure also the dc-bus voltage is kept at 680 volts and the grid voltage and current after compensation is in-phase.



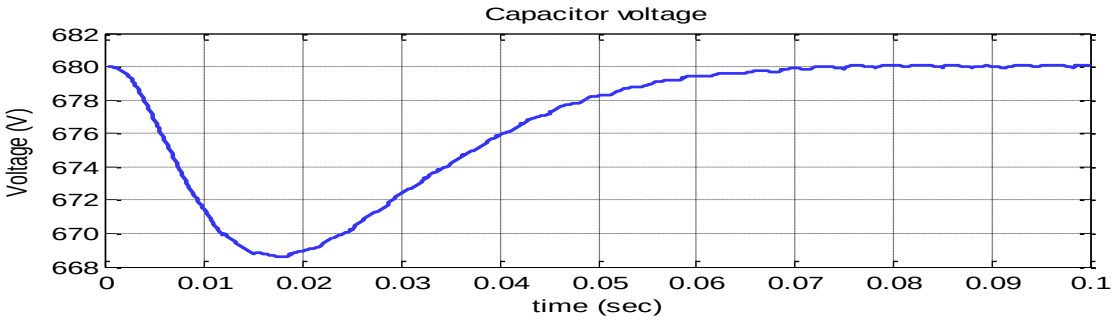
(a) Grid voltage and current after compensation



(b) Load current



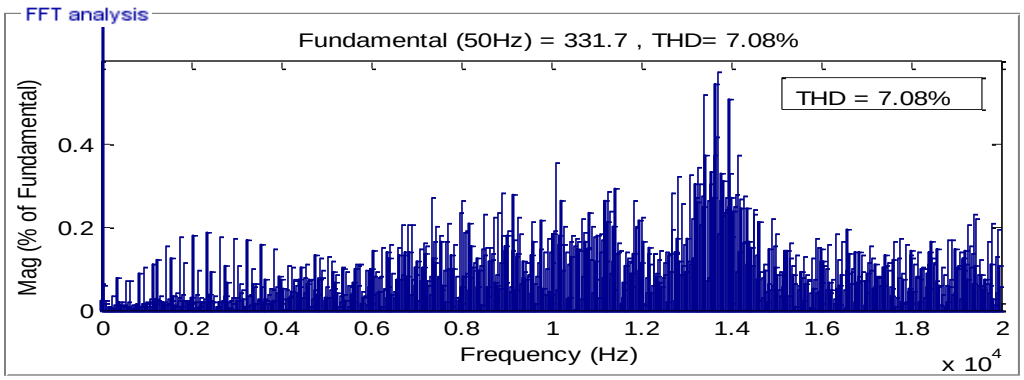
(c) Injected current



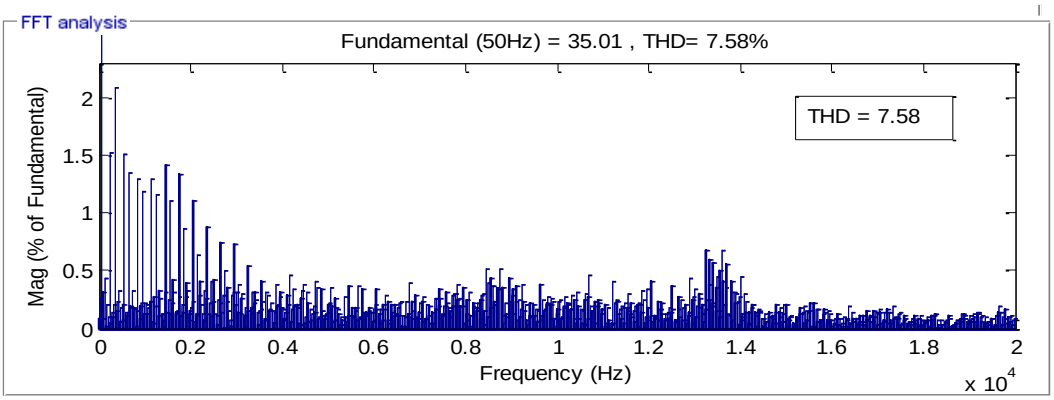
(c) dc-link voltage

Figure 3.15 Simulation results of DSTATCOM using SRF strategy

THD analysis is carried out using FFT analysis tool using Matlab/Simulink powergui interface. Figure 3.16 and 3.17 shows the THD analysis of DSTATCOM using IRPT algorithm and SRF strategy respectively.

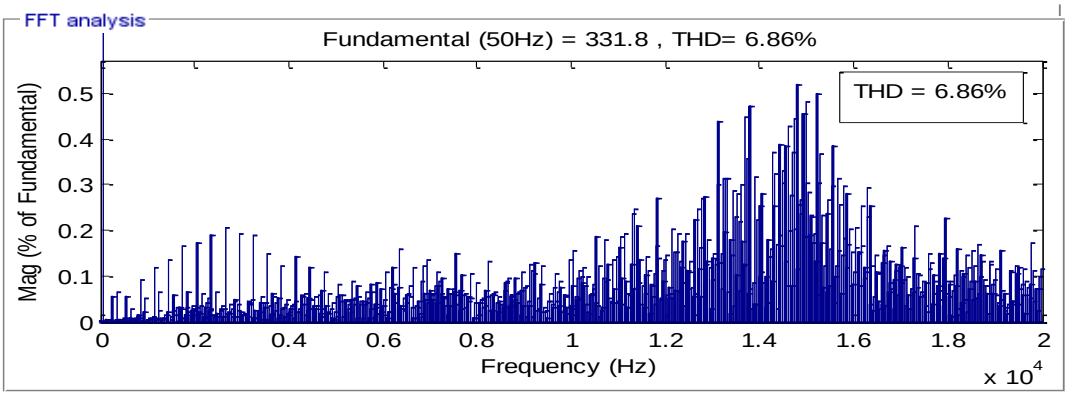


(a) Source voltage THD

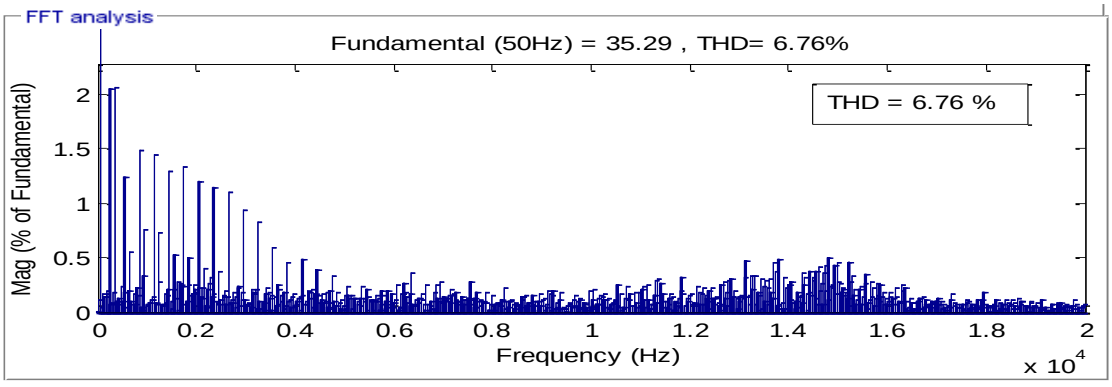


(b) Source current THD

Figure 3.16 Frequency spectrum of Source voltage and current (IRPT)



(a) Source voltage THD



(b) Source current THD

Figure 3.17 Frequency spectrum of Source voltage and current (SRF)

For the extraction of current reference, the most popular methods that are widely accepted in the DSTATCOM applications are IRPT and SRF methods. The FFT analysis shows that the total harmonic distortion of source voltage and current of the DSTATCOM using SRF method gives better results than using IRPT algorithm.

3.6 Summary

In this chapter, a detailed explanation of the basic principle and controller design of DSTATCOM is given. The mathematical derivation of both synchronous reference frame (SRF) strategy and the instantaneous reactive power theory (IRPT) have been demonstrated and the transformation equations for the Clarke's and Park's transformations were derived. A detailed idea about how the three phase quantities appear in the α-β and d-q plane was provided and this aided in understanding how the reactive and harmonic current reference can be generated using co-ordinate transformations. A detailed explanation of current and voltage controllers of the DSTATCOM is given and finally, the complete control structure is developed using various concepts developed. Here, the analysis is carried out using two-level VSI as it can extendable to multilevel inverter. The simulation studies helped in understanding the principle involved in the development of DSTATCOM and found that the reactive current compensation and harmonic filtering give favorable results. Harmonics may not be fully compensated due to the restrictions posed by the VSI that can generate voltages only in a time-averaged sense. THD analysis showed that d-q method achieved better harmonic compensation performance.

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Chapter 4

Modelling of Infinite Level Inverter (ILI)

4.1 Introduction

A single phase switched-mode dc-ac converter was introduced in 1998, which can address the limitations of existing VSI topologies. There has been a lot of active research on the switched-mode dc-ac converters utilizing dc -dc converter topology which can be used for various applications. This chapter introduces three-phase Infinite Level Inverter topology and its control to implement dc-ac conversion. Three-phase infinite level inverter is an extension of single phase Infinite Level Inverter. It can be of significant interest in the area of power electronics since a reliable and efficient system which produces minimum THD can be put into use in various applications. The ac voltage from the ILI can be controlled theoretically to any value between zero to infinity. This chapter is organized as follow

Theory of three-phase infinite level inverter topology is explained in section 4.2. Advantages of single Phase Infinite Level Inverter are briefed in section 4.3. Section 4.4 discussed the simulation and simulation results and the chapter is concluded in section 4.5.

4.2 Three-Phase Infinite Level Inverter topology

The working principle of three-phase infinite level inverter (ILI) can be demonstrated utilizing a single-phase infinite level inverter. Consider a single-phase infinite level inverter as shown in figure 4.1(a). The soul of this inverter is a dc-dc buck converter. This topology operates on variable duty ratio. The average output voltage V_o of this buck converter is the duty ratio (α) times the input voltage V_s, that is:

$$V_o = \alpha V_s \quad \text{.....(4.1)}$$

where V_s is the input dc voltage and α is the duty ratio. SPWM signal is used to trigger buck converter.

$$\alpha \equiv m * |\sin \omega t| \ldots\ldots\ldots\ldots\ldots\ldots \quad (4.2)$$

where 'm' is the modulation index ratio. Now:

$$V_o = m * Vs * |\sin \omega t| \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (4.3)$$

The H-bridge in the ILI circuit works in synchronization with the rectified sine wave reference to unfold the buck output voltage at fundamental voltage reference. The output phase voltage of a single phase converter with peak amplitude of dc source V_s is given by:

$$V_{ac} = m * Vs * |\sin \omega t| \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.4)$$

If the input voltage V_s of the inverter is kept constant and the duty ratio is varied by using fully rectified sine PWM technique in which a fully rectified sine wave is compared with a high frequency triangular pulse (the frequency of the carrier triangular pulse is decided as required by the switching frequency). This technique generates a pulse width modulated rectified sine wave output across the buck capacitor as shown in figure 4.1(b). The inductor and capacitor of the buck circuit cancel all the high frequency elements in the output. The ac output rectified voltage of this converter is unfolded into a sinusoidal wave by H-bridge. It is switched at the fundamental frequency to unfold the rectified sine wave into a sinusoidal waveform as shown in figure 4.1 (b). The output voltage now has infinite levels depending on the switching frequency. Three such single phase inverters are joined and gated in such a way that the output voltage waveform is 120° out of phase with respect to each other. This output voltage is a high quality sine wave with reduced harmonic content as compared to the classical voltage source inverter.

4.3 Advantages of single Phase Infinite Level Inverter

1) In this inverter, out of five switches in a phase, a single switch is operating at higher frequency, switching losses are considerably low, and therefore this topology can be recommended for higher frequency operation.

2) The H-Bridge circuit of this topology operates at low frequency (say 50Hz) so this topology has safe delay interval and avoids the problem of short circuit. Also, because of the inductor in series with Vs, no shoot through issue.
3) In this topology, the filter capacitor can be of dc type such as polyester capacitor that is small in size and cost effective than that of capacitors used in ac circuits for the same capacity as demanded by the classical bridge type inverter configurations.
4) In this topology, the advanced control techniques such as current mode control, digital sampling control, and sliding mode control, etc. that are proposed to implement on dc-dc converters can be directly used. As a result, a better dynamic performance can be attained.

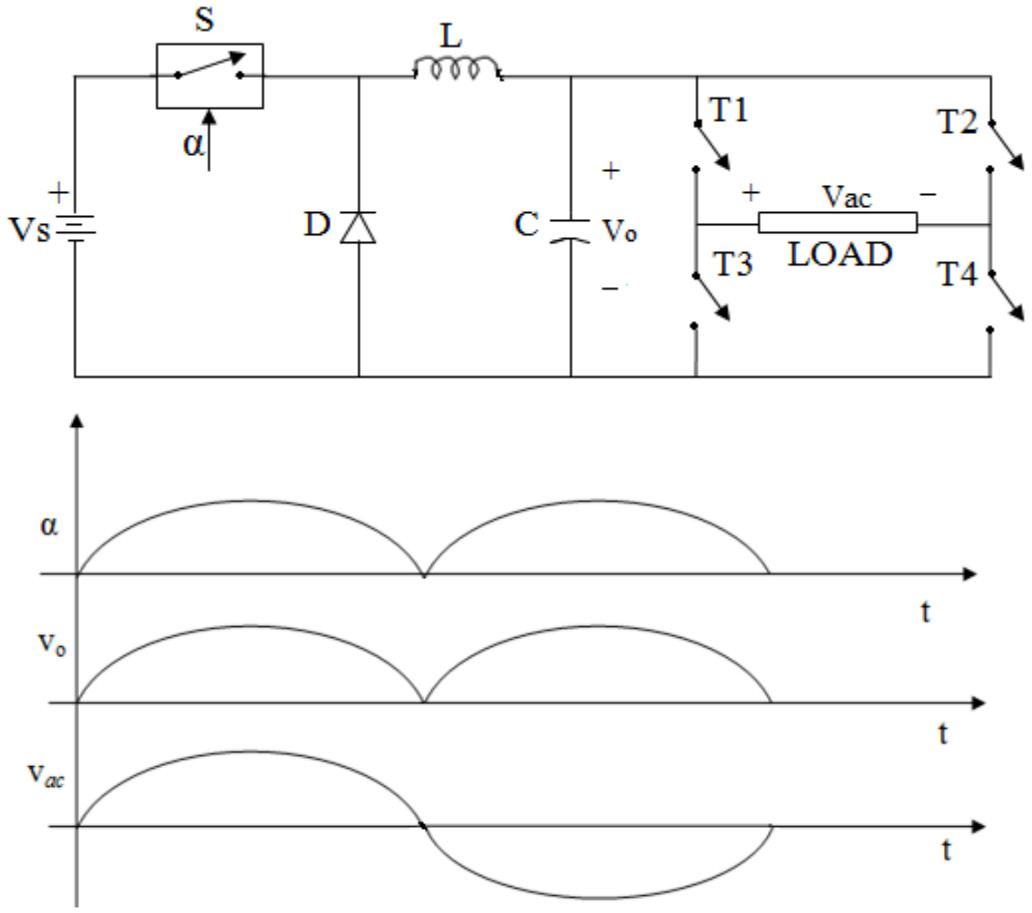

Figure 4.1 (a) Single-phase ILI circuit (b) Duty ratio (α), average output voltage wave form and voltage across the load

The three-phase output voltages of ILI with unity modulation index ratio are given by the equations:

$$V_{oa} = \alpha_a V_i \text{.....(4.5)}$$

$$V_{ob} = \alpha_b V_i \text{.....(4.6)}$$

$$V_{oc} = \alpha_c V_i \text{.....(4.7)}$$

where α_a, α_b, α_c and V_{oa}, V_{ob}, and V_{oc} are duty ratios and output phase voltages of phase a, phase b and phase c respectively. These are gated at a phase angle delay of 120^0 with respect to each other, thus:

$$\alpha_a \equiv m|\sin \omega t| \text{.....(4.8)}$$

$$\alpha_b \equiv pulseof V_m |\sin(\omega t - 120)| \text{.....(4.9)}$$

$$\alpha_c \equiv pulseof V_m |\sin(\omega t - 240)| \text{.....(4.10)}$$

Take modulation index ratio = 1, the output voltage equations will be as given below:

$$V_{oa} = V_i |\sin \omega t| \text{.....(4.11)}$$

$$V_{0b} = V_i |\sin(\omega t - 120)| \text{.....(4.12)}$$

$$V_{oc} = V_i |\sin(\omega t - 240)| \text{.....(4.13)}$$

From these equations, it is clear that the switching pattern produces a rectified sine wave across the output filter condenser 'C' of the buck converter. These voltages are displaced with 120^0 with respect to each other and with a peak magnitude of V_i. The number of switching instants, i.e. the number of levels in the voltage waveform across the capacitor depends on the carrier frequency as set in the fully rectified sine PWM generator. The rectified sinusoidal waveforms available across the capacitor are then converted into sinusoidal output voltages to be made available across the load using H-bridge configuration operating at a lower frequency say 50Hz. As a result the switching losses in H bridge devices are neglected as compared to the losses in the high frequency semiconductor switches in the buck converter.

The switching of H-bridge switches is done with respect to their corresponding reference sine waveforms. The diagonal pairs of switching devices (T_1, T_4) and (T2, T3) are switched on and off with respect to their fundamental reference waveform. For instance, at time t = 0, switches (T_1, T_4) are switched on and continues till time t = T/2. Switches (T2, T3) are switched on from time t = T/2 to the end of one time period t = T and the switching continues.

Unfolded sine waves are,

$$V_{oa} = V_i \left|\sin \omega t\right| \text{.....(4.14)}$$

$$V_{oa} = V_i \sin(\omega t - 120) \text{.....(4.15)}$$

$$V_{ob} = V_i \sin(\omega t - 240) \text{.....(4.16)}$$

The equations (4.14 to 4.16) represent the phase voltages which are 120^0 out of phase with each other and the peak amplitude is same as that of input DC voltage. These voltages are a good quality sine wave with very low harmonic contents. This inverter acts as a three-phase voltage source inverter providing a perfect balanced three-phase sinusoidal voltage waveform if it is applied to a three-phase balanced resistive load. Hence neutral connection is optional and could operate as 3Φ, 3 wire network. The three-phase ILI is shown in figure 4.2.

From the balanced phase to neutral voltage equations (4.14-4.16), the line-line voltage equations are,

$$V_{La} = \sqrt{3} \times V_i \sin(\omega t + 30) \text{.....(4.17)}$$

$$V_{Lb} = \sqrt{3} \times V_i \sin(\omega t - 90) \text{.....(4.18)}$$

$$V_{Lc} = \sqrt{3} \times V_i \sin(\omega t - 210) \text{.....(4.19)}$$

These line voltage equations (4.17 to 4.19) are 30^0 phase advanced and √3 times the magnitude of its corresponding phase voltages. In order to achieve a basic Line to Line RMS voltage of 400 Volts, 50 Hz, the input DC voltage requirement for three-phase ILI is given by:

$$\sqrt{3} * V_i = 400 * \sqrt{2}$$

$$V_i = 325 \text{ V DC}$$

This DC voltage is almost half the DC voltage required by the traditional PWM inverter topologies which are shown in table I. The equation of the Line-Line voltage is given by:

$$V_{l-l} = \left(\sqrt{3/2}\right) \times V_i = 1.23V_i \text{.....(4.20)}$$

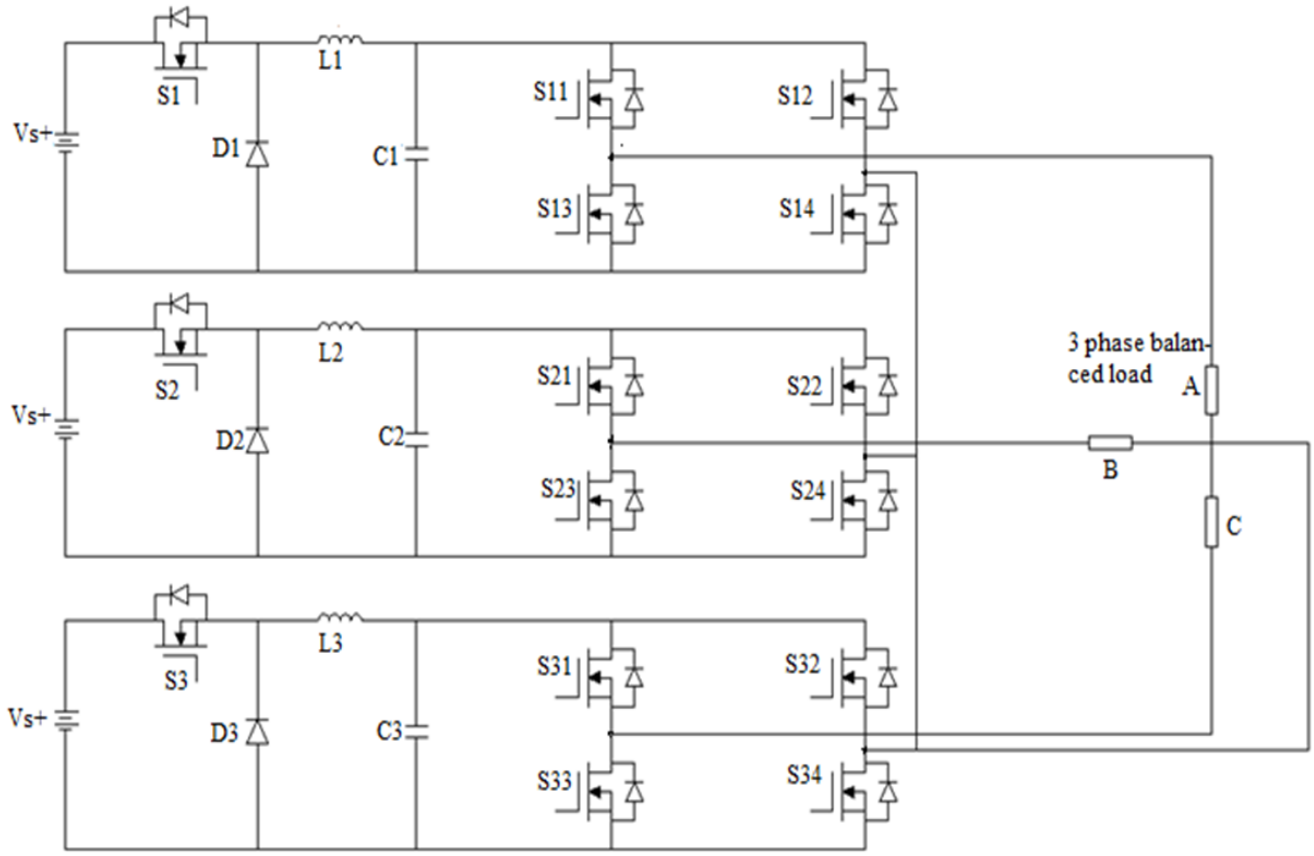

Figure 4.2 Circuit diagram of three-phase infinite level inverter (ILI) topology

This Line-Line fundamental rms voltage is 123 percent of its dc voltage input (V_i). Therefore the ILI has the lower dc voltage input to produce a three-phase rms voltage of 400 V. Which means this topology requires just 325V dc to produce a Line-Line sinusoidal voltage wave of 400 V.

Table 4.1 Comparison of different inverter topologies with the proposed infinite level inverter

Type of inverter	Line Voltage V_L &phase voltage *Vp*	Dc Voltage input V_s	Times the proposed inverter	Characteristics
Classical VSI	$V_{L=}$ 0.78 V_s $V_{p=}$ 0.45 V_s	512 V	1.58	Large THD, complicated filter design
SPWM	$V_{L=}$ 0.613 V_s $V_{p=}$ 0.353 V_s	654V	2.01	High input voltage, voltage stress, power loss
Space-Vector PWM	$V_{L=}$ .707V_s $V_{p=}$ 0.408 V_s	564V	1.74	High input voltage, voltage stress, power loss
Infinite Level Inverter	$V_{L=}$1.24 V_s $V_{p=}$ 0.707 V_s	325V	1	Very low THD negligible power loss & device stress

In addition to the advantages of single phase ILI that are also true for three phase ILI, following benefits are there in case of three phase ILI.

- The switching loss is reduced substantially. This is because unlike the PWM inverters where six switches working at carrier frequency, only three switches of this three phase ILI work at carrier frequency and the rest of the switches are assigned to operate on fundamental frequency.
- The H-Bridge switches are soft switched (ie; switching action takes place at the zero voltage condition). While in other pulse width modulated converters, all the six switching

devices are hard switched which result heavy switching loss. Table 4.2 depicts the comparison of switching losses of different inverter technologies.

- Since hard switching generates a severe issue if the dc voltage input is above 500 volts and switching devices need to be replaced from power MOSFETs to IGBTs owing to the complexity in large power ratings of MOSFETs and reverse recovery issue of body diode. Consequently, in conventional PWM inverters, the reduced power losses and high switching speed properties of MOSFETs cannot be used. Furthermore, IGBTs result in high switching power loss owing to the following;

  - Reduced speed of triggering because of higher voltage and current overlap time and hence bigger overlap area.
  - Higher tail current during turn off period results in high power losses.

  In this proposed inverter, owing to considerably lower input DC voltage, these problems can be avoided and has

- Very high utilization of DC link. For instance, in the proposed inverter, the input DC voltage needed is only 325 volts to acquire a Line-Line rms voltage of 400 volts and this is only half of the input required for three-phase sine PWM inverter (SPWM requires 654V DC to get 400V AC) and 0.576 times Vs for 3rd harmonic injection or space vector PWM (SVPWM). Comparison is shown in table-4.1.
- Minimized voltage stress across the switching devices that results in superior reliability of the system.
- Shoot-through menace is neglected in this topology and thus there is no dead time requirement.
- The proposed inverter has same number of active and passive components for infinite number of voltage levels whereas in multi-level inverters, number of active and passive components increases as the number of voltage level increases.
- Higher number of voltage levels in output voltage waveform lowers the harmonics content to a great amount. The FFT analysis show that the THD is below 2%. Thus the inverters can be employed in critical application area such as hospitals and airports [IEEE std 519].
- Even though the conduction loss is large because of the extra switches per phase, the overall losses will be low, thereby enhancing the efficiency.

Table 4.2 Comparison of switching losses of various inverter technologies

No of active switches	Switching Loss		Conduction loss
	Carrier frequency	Fundamental frequency	
SPWM inverter	6	-	3
Proposed ILI	3	6 (soft switched at ZV)	9

4.4 Simulation and simulation results

The simulink model of three-phase ILI topology (shown in Figure.4.2) is implemented and simulated in MATLAB / Simulink environment with R, RL, and Star connected loads. For obtaining an rms Line-Line voltage of 400 volts, 50 Hz AC output, buck converter parameters considered are given in the table 4.3.

Table 4.3 Simulation parameters

VARIBLES	VALUES
Inductance	10 mH
Capacitance	0.4µF
Load	100Ω, 1mH,star connected.
DC Bus voltage	325 volts
System frequency	50 Hertz
Switching frequency	10 kilo Hertz

Here, the reference signal has peak amplitude of 325 volts and fundamental frequency of 50Hz. Figure 4.3 shows the simulation results of three-phase ILI with star connected RL load at steady state at an operating frequency of 50 Hz. In figure 4.3 (a), the average output voltage across buck capacitor, with a peak value of 325 V is shown. The Line-Line rms voltage is 400 volts AC with

570 volts peak (figure 4.3 (b)). The output rms voltage of each phase is 230 volts with a peak value of 325 volts (figure 4.3 (c)). The line voltages are 30º phase advanced with respect to corresponding phase voltages which are shown in figure 4.3 (e). Line current through star connected load is a high quality sinusoid with very low ripple content as shown in figure 4.3 (d). As per IEEE 519 standard, harmonic limit on voltage is 5% for THD. FFT analysis is done in MATLAB/ Simulink using fast Fourier tool and the line voltage THD is less than 2% .This indicates the quality of output voltage. The obtained simulation results are in accordance with the proposed concept.

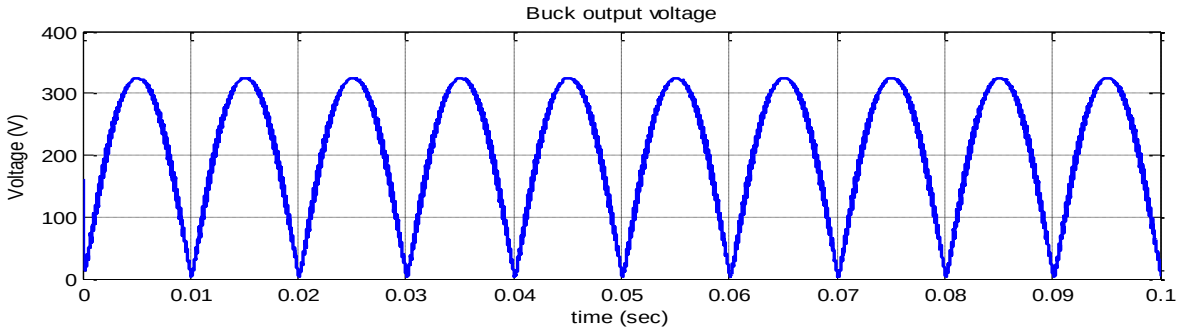

Figure 4.3 (a) Output voltage across buck capacitor

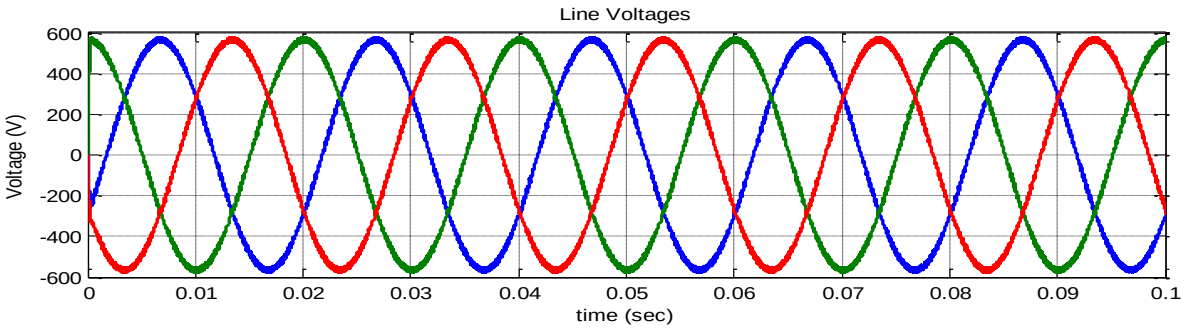

Figure 4.3 (b) Three-phase line voltages of ILI.

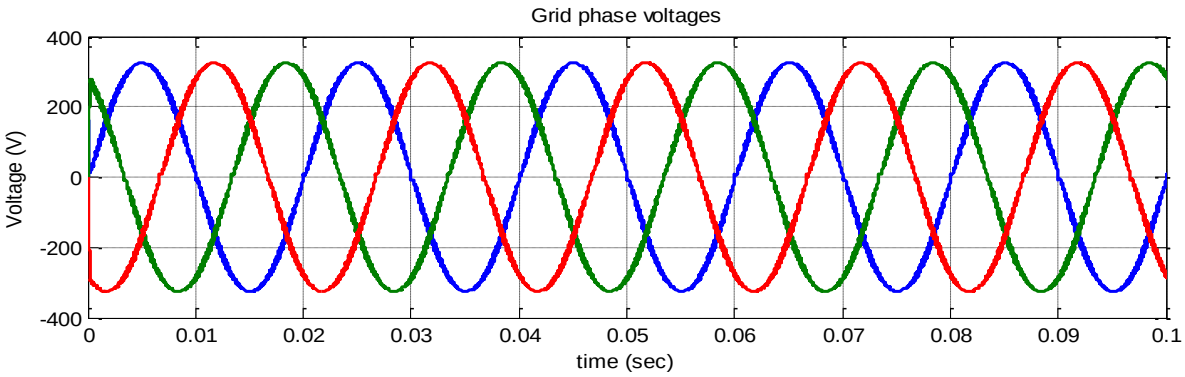

Figure 4.3 (c) Phase voltages of three-phase ILI.

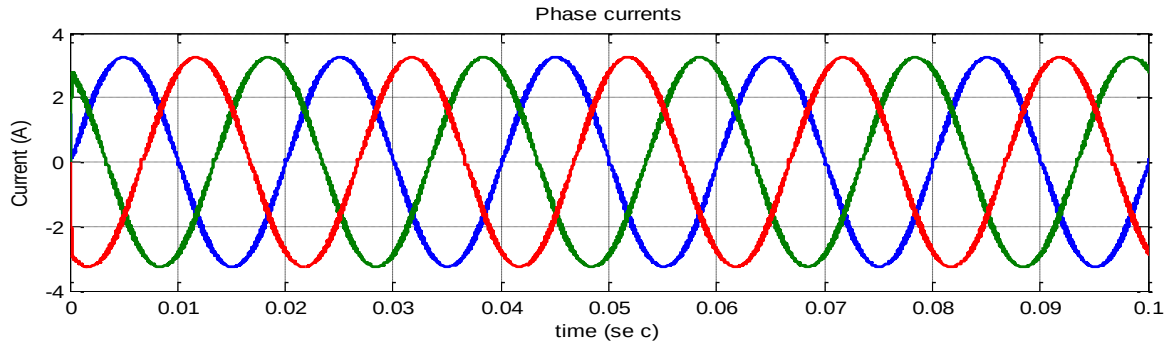

Figure 4.3 (d) Phase currents of three-phase ILI.

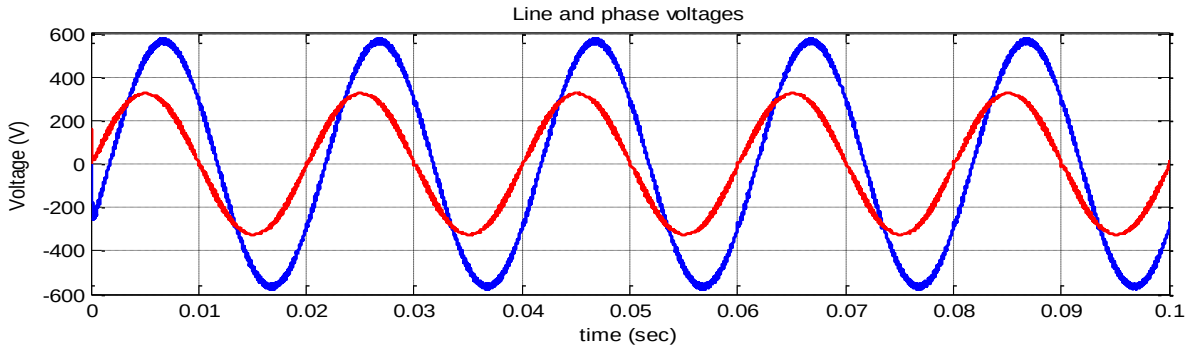

Figure.4.3 (e) Line voltage & Phase voltage of three-phase ILI.

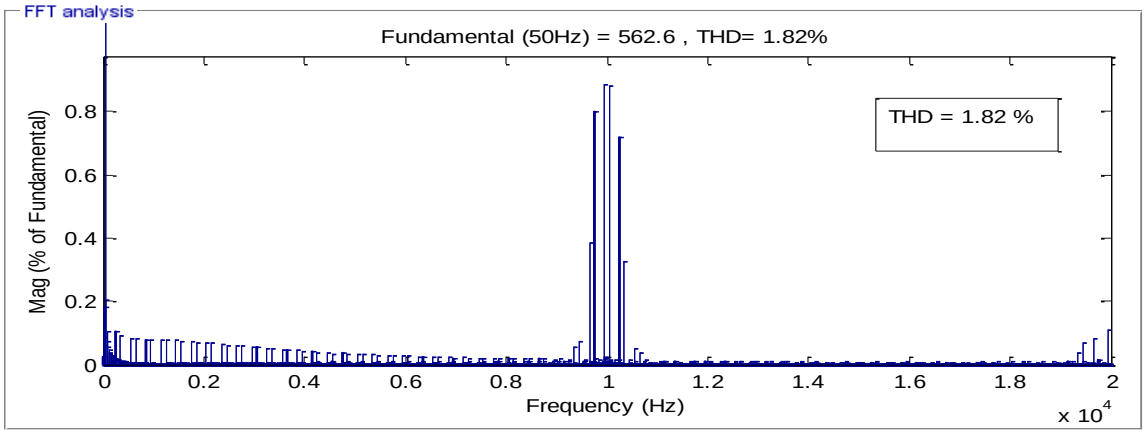

Figure 4.4 (a) Frequency spectrum of source voltage using FFT (RLC load).

Figure 4.4 (a) and figure 4.4 (b) show that the THD analysis using FFT of source voltage and source current for RLC load. The THD analysis of source voltage and source current for RL load is shown in the figures 4.5 (a) and (b) respectively. Also, the FFT analyses to find THD for different kinds of load are shown in the table 4.4. From these, it is evident that whatever be the load conditions, total harmonic distortion of the source voltage is lower than 2 % and that of source current THD is very less. For RL load, the source current THD is less than 1 %.

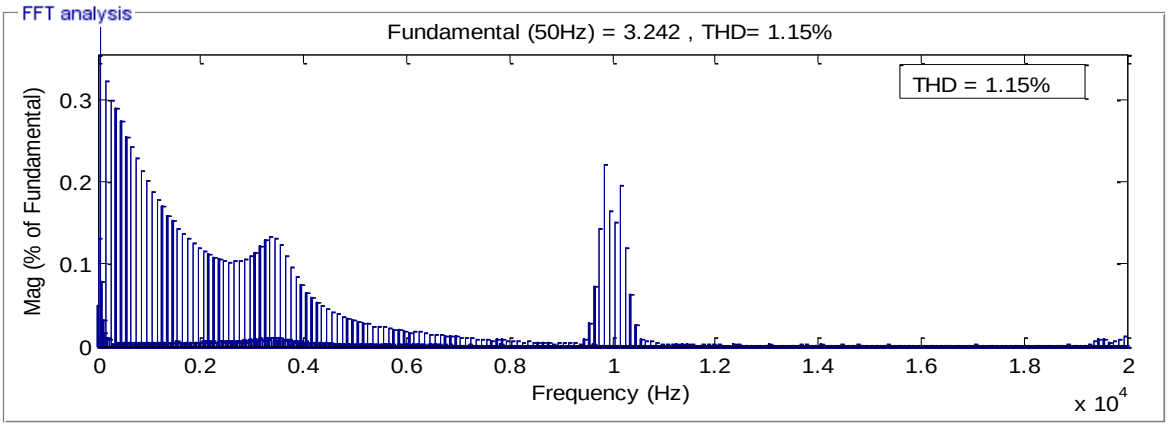

Figure 4.4 (b) Frequency spectrum of source current using FFT analysis (RLC load).

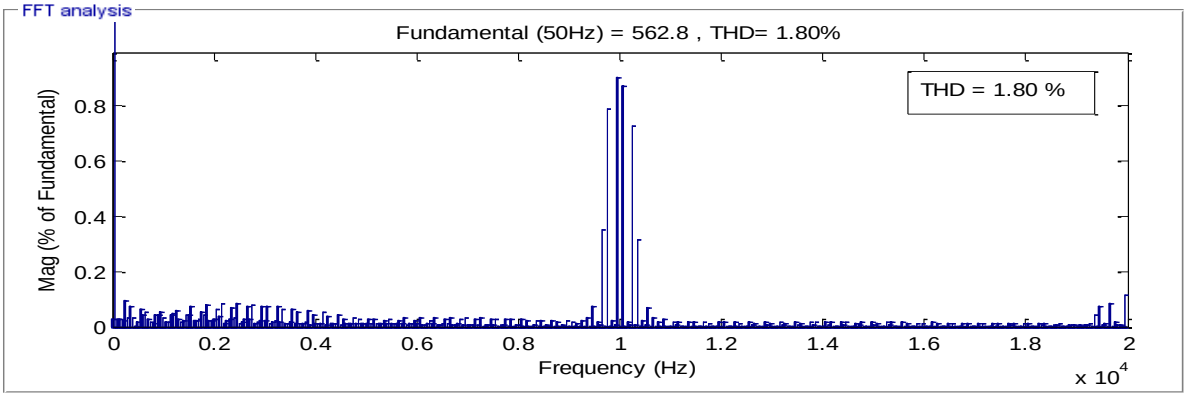

Figure 4.5 (a) Frequency spectrum of source voltage using FFT analysis (RL load).

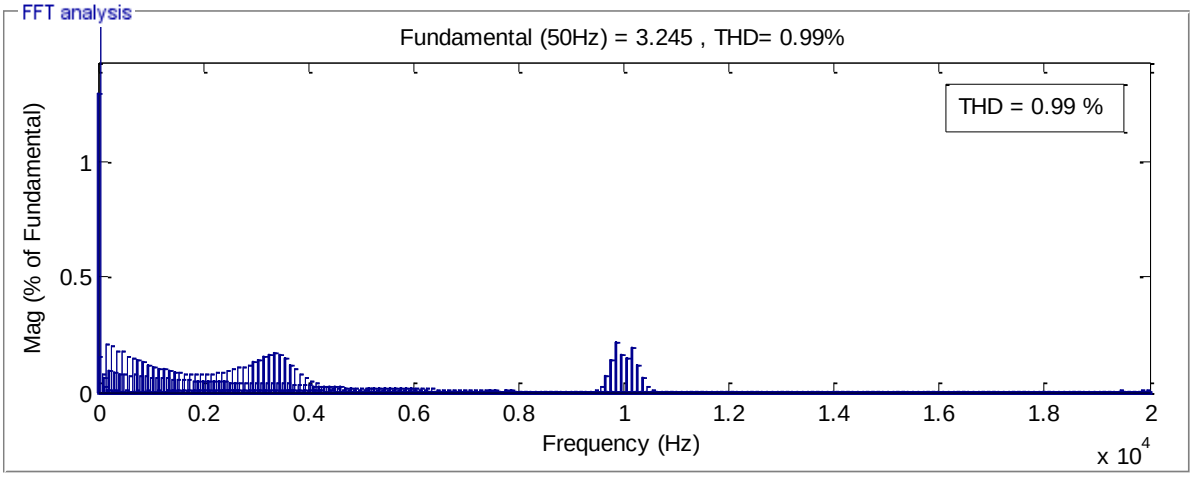

Figure 4.5 (b) Frequency spectrum of source current using FFT analysis (RL load).

Table 4.4 THD analysis for different loads

Load	Voltage THD (%)	Current THD (%)
R	1.81	1.32
RL	1.82	0.99
RC	1.83	1.20
RLC	1.81	1.15

4.5 Summary

In this chapter, the mathematical modeling and operating principle of three phase infinite level inverter is explained. It has numerous advantages over the traditional bridge and PWM inverters. The inverter model is demonstrated in the MATLAB /SIMULINK environment. The three-phase infinite level converter technique is a switch mode inverter based on minimizing the number of active switches and passive components used as compared to multilevel inverters. The output ac voltage can be any value between zero and infinity. It is also obvious that the fundamental output voltage obtained from the proposed infinite level inverter (ILI) requires less input DC voltage with very high DC-link utilization. This topology helps in reducing the switching losses and the analysis presents a very low value of THD. FFT analysis of voltage waveform from three-phase ILI shows that the source voltage and current THD for different types of load are less than 2% at high switching frequencies.

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Chapter 5

Infinite Level Inverter as DSTATCOM

5.1 Introduction

Multi-Level Inverter topology is a boon to power system industries. In the present scenario, the power industries need high voltage and high quality sinusoidal voltage and current waveforms. These demands can be achieved by multi-level Inverter topologies. These are widely used in moderate or high voltage electrical network to minimize the voltage stress across switching devices. However, it requires numerous dc sources. The major topologies of MLIs for DSTATCOM applications have been presented in the literature.

This chapter discusses the application of three-phase, infinite level voltage source inverter (ILI) topology as DSTATCOM. The ILI topology and its working principle are explained in detail in the previous chapter. This topology has an infinite number of voltage levels depending on the carrier frequency used. The main goal of this work is to eliminate harmonics by a novel inverter circuit topology for inverter feeding current at the point of common connection. This topology demands lower dc-link voltage. Performance of this DSTATCOM is analyzed with SRF strategy. The current controller used for the generation of pulses is constant band hysteresis current controller (HCC). The DSTATCOM configuration is developed in the MATLAB /SIMULINK environment using Sim power systems block set. The power quality compensation in terms of reactive power compensation and harmonic elimination of the ILI based DSTATCOM is analyzed. This chapter is organized as follow

Working principle of three phase ILI based Dstatcom is explained in section 5.2. System description is explained in section 5.3. Control strategy for ILI based DSTATCOM is explained in section 5.4. Voltage Controllers for this ILI based Dstatcom are briefed in section 5.5. Section

5.6 discussed the simulation and simulation results of ILI based Dstatcom. Comparison of this with the traditional VSI is given in section 5.7. The chapter is concluded in section 5.8.

5.2. Working principle of the three phase ILI based DSTATCOM

A DSTATCOM is a shunt connected voltage source converter (VSC) which is tied to the distribution network. A distribution system is usually not designed for connecting electricity generation units. Since distribution systems is generally a radial or loop design, the power flow in a distribution line is normally unidirectional and no or little redundancy exists. The main purpose of the DSTATCOM is to inject a nearly sinusoidal current of variable amplitude, at the point of common coupling (PCC). This injected current is almost in quadrature with the line voltage, thereby emulating an inductive or a capacitive reactance at the point of common coupling with the distribution network. Here the three-phase infinite level inverter acts as the VSC to realize the DSTATCOM with the reference current extraction algorithm. The reference currents are compared with the inverter currents to generate necessary switching pulses.

The ILI is a power electronic circuit that generates a sinusoidal voltage with any desired amplitude, frequency, and phase angle. Figure 5.1 represents the three-phase infinite level inverter (ILI) as DSTATCOM which is an important application of ILI. It consists of an ILI, a capacitor to store energy, and an interfacing reactor. When a dc voltage supply is connected to the input of the ILI-DSTATCOM, the inverter is triggered to produce the required voltage output. The ILI can produce three alternating voltages from a dc source by means of power electronic switches. These voltages are in phase with the ac distribution network and fed to the PoC by means of current injecting transformer and coupling reactor. By properly adjusting the output voltage amplitude of the DSTATCOM, an effectual regulation of reactive power transfer between the DSTATCOM and the ac distribution network can be achieved. This topology restricts the use of a finite number of voltage levels. The number of voltage levels in a cycle depends on the switching frequency. In this inverter, as the voltage levels increase, the number of

active and passive components will not increase. With this converter technique, the injected current harmonics can be made near to zero. Harmonics can be said to be dependent on the difference between the instantaneous value of the reference voltage and the voltage levels between which switching take place. Here, the difference between the instantaneous voltage

reference and the levels of voltage between which the switching takes place is theoretically zero. The D-STATCOM controller continuously observes the load voltages and currents and estimates the amount of compensation demanded by the ac network under different operating conditions. It serves three clear motives:

- Regulation of voltage and reactive power compensation
- Power Factor (PF) correction
- Current harmonics elimination

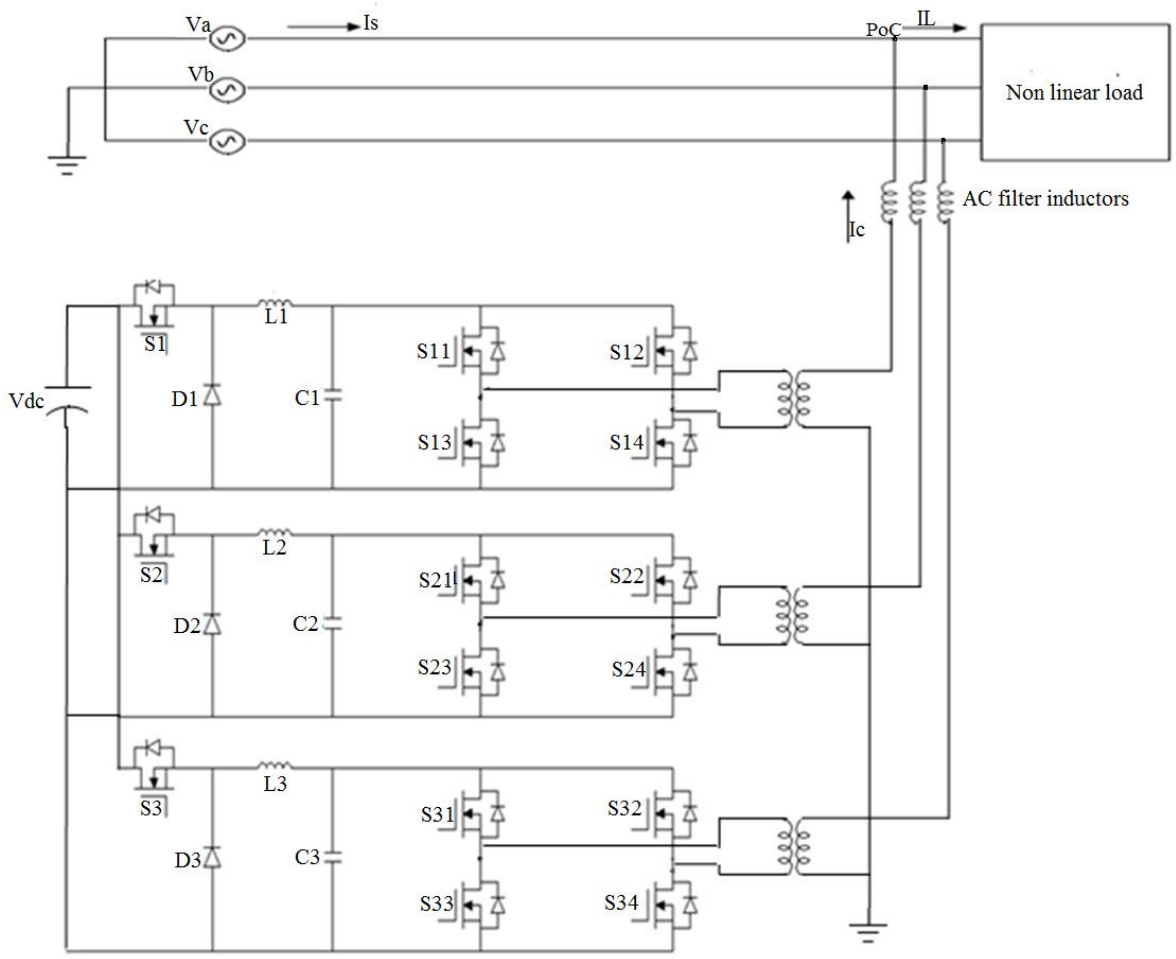

Figure 5.1 Three-phase ILI as DSTATCOM

5.3 System description

The three load current components of a three-phase non-linear load are real, imaginary and harmonic components. Sum of these three current components gives the integral instantaneous power absorbed by nonlinear load and can be written as follows;

$$P_t = p_r + q + p_h \quad \text{.....(5.1)}$$

where p_t, p_r, q, and p_h stand for instantaneous, active, reactive, and harmonic powers respectively and $p_r + p_h$ is the total real power drawn by the non-linear load. Here, the job of the ILI is to supply the imaginary and harmonic current components required by the load. This is achieved by proper control of the system. So the grid needs to supply only the real component. The real and imaginary power delivered by the grid is given by;

$$P_s = p_r \text{.....(5.2)}$$
$$q_s = 0 \text{.....(5.3)}$$

where p_s and p_r are source and real powers respectively

Imaginary power absorbed by the non-linear load is;

$$q_L = q_f + q_h \text{.....(5.4)}$$

where q_f , and q_h are fundamental and harmonic imaginary powers respectively

Active and imaginary power delivered by DSTATCOM is;

$$P_D = p_h + p_L \text{.....(5.5)}$$
$$q_c = q_f + q_h \text{.....(5.6)}$$

where p_L is the loss component of the DSTATCOM.

5.4 Control strategy for ILI based DSTATCOM

The operating function of the inverter is greatly depends on the performance of the selected current control algorithm. Rotating reference frame (d-q) based technique offers higher accuracy than stationary reference frame based technique. This controller adapts a phase locked loop to synchronize the three-phase voltages at the inverter output with the grid. The reference current signals are given to the current controller to produce pulses for the inverter operation. The goal of

the control strategy is to keep fixed voltage amplitude at the point of connection where a sensitive nonlinear load is affixed. During the operation, the DSTATCOM continuously observes the network primary terminal and differentiates it with a reference signal. It then injects the necessary voltage and harmonic currents to compensate for the distortion caused by the non-linear load. Thus ILI can act as an ideal DSTATCOM to avert interfering loads from disturbing the remaining part of the distribution network. In the present study, hysteresis current controller is used to control the VSI. The hysteresis controller requires current references for control. Once the current references are generated, the inverter along with the choke tries to follow the current reference. The connection between inverter and grid through choke, i.e DSTATCOM is shown in figure 5.2. Thus, it is clear that the inverter along with the choke must be the 'plant'. So, the transfer function of the plant can be arrived at by using the Inverter – Choke – Grid setup (R-L circuit) shown in figure 5.3.

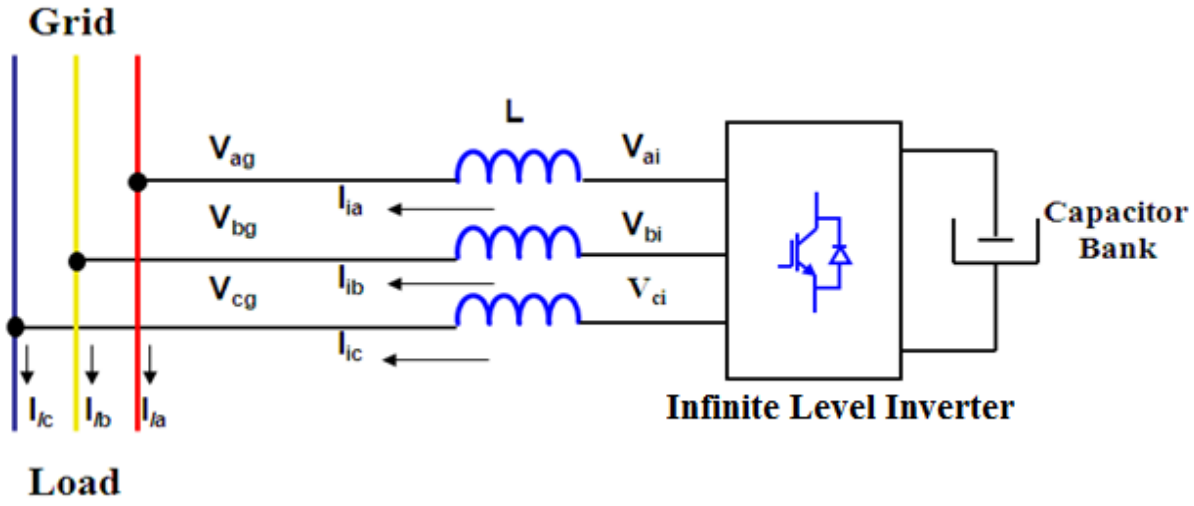

Figure 5.2 Schematic of DSTATCOM

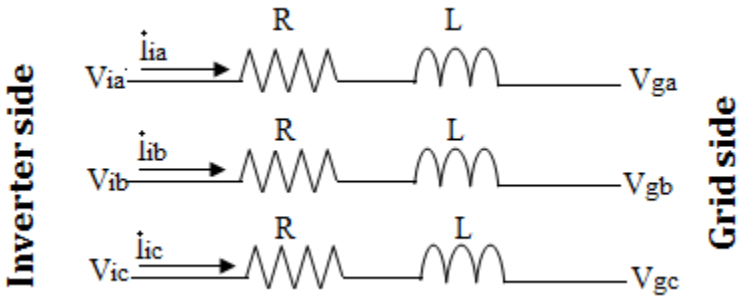

Figure 5.3 Inverter - choke - grid setup as DSTATCOM's plant

The symbols in figure 5.3 can be expanded as follows,

v_{ia}, v_{ib}, v_{ic} - Converter side instantaneous voltages (in volts), where

$(v_{ia} = v_{ai}, v_{ib} = v_{bi}, v_{ic} = v_{ci})$. and $(v_{ga} = v_{ag}, v_{gb} = v_{bg}, v_{gc} = v_{cg})$

i_{ia}, i_{ib}, i_{ic} - Converter currents passing through the inductor (in amperes).

v_{ga}, v_{gb}, v_{gc} - Source side instantaneous voltages (in volt).

L, R - Per phase inductance (in Henry) and resistance (in ohm) of the choke.

Since the current references in the SRF strategy are in the d-q plane, the equations are first written in the *R-Y-B* plane and then they are transformed to the $\alpha\beta$ −plane and subsequently to the *d-q* plane. This helps in deriving the controller transfer function in the *d-q* plane so that it can be directly used in the practical implementation.

Applying KVL to the R-L circuit shown in figure 5.3,

$$v_{ia}(t) - v_{ga}(t) = R * i_{ia}(t) + L * \frac{d_{ia}(t)}{dt} \text{.....(5.7)}$$

$$v_{ib}(t) - v_{gb}(t) = R * i_{ib}(t) + L * \frac{d_{ib}(t)}{dt} \text{.....(5.8)}$$

$$v_{ic}(t) - v_{gc}(t) = R * i_{ic}(t) + L * \frac{d_{ic}(t)}{dt} \text{.....(5.9)}$$

Using Clark's transformation, the voltage equations corresponding to α-β coordinates can be written as

$$\begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \text{.....(5.10)}$$

and

$$\begin{bmatrix} a \\ b \\ c \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \alpha \\ \beta \end{bmatrix} \text{.....(5.11)}$$

The voltage equations (5.7 to 5.9) can be expressed in α-β coordinates as

$$v_{i\alpha} - v_{g\alpha} = R * i_{i\alpha} + L * \frac{di_{i\alpha}}{dt} \text{.....(5.12)}$$

$$v_{i\beta} - v_{g\beta} = R * i_{i\beta} + L * \frac{di_{i\beta}}{dt} \text{.....(5.13)}$$

Applying the definition of space vector,

$$\bar{V} = v_{\alpha} + jv_{\beta} \text{.....(5.14)}$$

$$\bar{V}_i - \bar{V}_g = R * \bar{I}_i + L * \frac{d\bar{I}_i}{dt} \text{.....(5.15)}$$

By applying the Park transformation, the voltage equations in α-β coordinates can be transformed into d-q coordinates as

$$v_{id} = R * i_{id} + L\frac{di_{id}}{dt} - \omega L * i_{iq} + \left|\bar{V}\right| \text{.....(5.16)}$$

$$v_{iq} = R * i_{iq} + L\frac{di_{iq}}{dt} + \omega L * i_{id} \text{.....(5.17)}$$

where

$$\left(v_{gd} + jv_{gq}\right) = \left|v_{\alpha} + jv\beta\right| = \left|\bar{V}\right| \text{.....(5.18)}$$

From the above equations, the plant transfer function can be derived in terms of direct and quadrature axis that is shown in the figure 5.4.

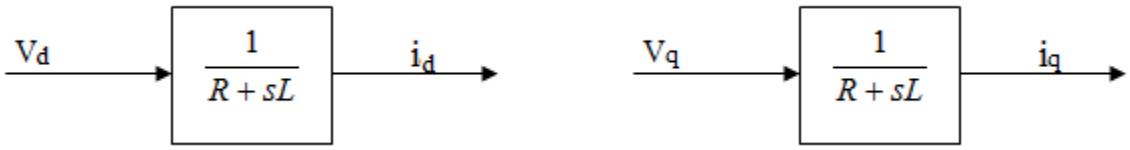

Figure 5.4 plant transfer function in d-q plane

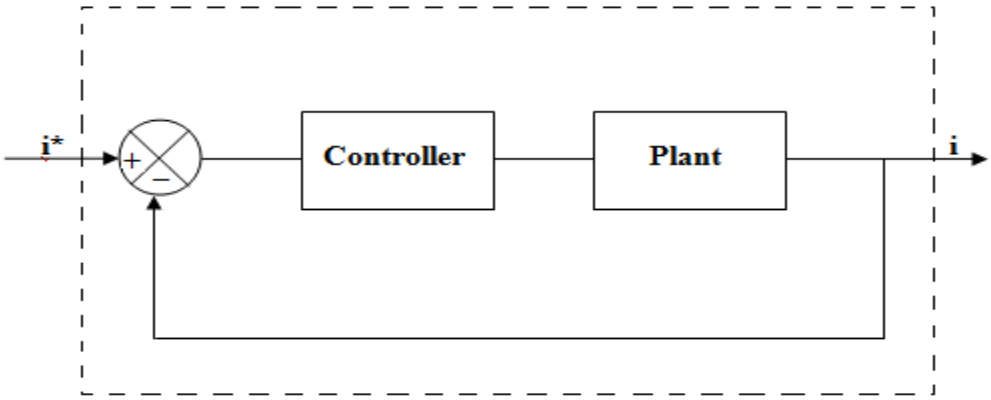

Figure 5.5 Structure of current controller

Figure 5.5 gives the block diagram demonstration of a familiar control system structure. Knowing the plant transfer function $G_p(s) = \frac{1}{R + sL}$, the transfer function of the current controller can be easily obtained. Assuming the whole system as a first order LPF for the sake of simplicity, the transfer function of the system is given by

$$\frac{G_c(s) \times \left[\frac{1}{R + sL}\right]}{1 + G_c(s) \times \left[\frac{1}{R + sL}\right]} = \frac{1}{\tau * s + 1} \quad \text{.....(5.19)}$$

$$\Rightarrow \frac{G_c(s) * \left[\frac{1}{R + sL}\right]}{1 + G_c(s) * \left[\frac{1}{R + sL}\right]} = \frac{\frac{1}{\tau \times s}}{1 + \frac{1}{\tau \times s}} \quad \text{.....(5.20)}$$

$$\Rightarrow G_c(s) * \left[\frac{1}{R + sL}\right] = \frac{1}{\tau \times s} \quad \text{.....(5.21)}$$

$$\Rightarrow G_c(s) = \frac{L}{\tau} + \frac{\left(R/\tau\right)}{s} \quad \text{.....(5.22)}$$

5.5 Voltage Controllers

In the DSTATCOM application of ILI, the goal is to make the ILI continuously track and supply the reactive and harmonic currents required by the load. This calls for the use of a current controller. Theoretically, this alone is sufficient. But practically, the voltage in the dc bus capacitor generally reduces continuously if there is no controller in place to maintain it at the desired value.

The reason for this is that there will be losses at the switching devices (conduction loss and switching loss) and power dissipation at the choke that connects the inverter to the grid (due to the small but finite resistance associated with it). The only source of energy being the dc-link capacitor, it is obvious that it should lose some voltage to supply for the energy losses in the network. Therefore, there is a need for a voltage controller to maintain the dc-link voltage at a desired value (or equivalently - to meet the active power requirement of the system). Hence, the control strategy uses a proportional integral (PI) controller to control the dc-link voltage of the DSTATCOM. The dc-link voltage of the DSTATCOM is sensed and compared with the reference quantity and the error is given to the PI regulator.

Figure 5.6 gives the block diagram demonstration of the control technique that involves a dc bus voltage regulator, reference current generator, a current regulator and pulse generator. The SRF strategy is a famous method used to generate current reference. It first transforms voltages and currents from a-b-c to α-β frames and then transforms α-β coordinates into d-q frame as shown. It may be noted that in the above compensation technique, the filter employed is the low pass filter. The function of the low pass filter is to block the dc element and the cut-off frequency of this device is selected as 10 Hz. The output of this filter is dc and therefore it will not suffer any amplitude or phase distortion.

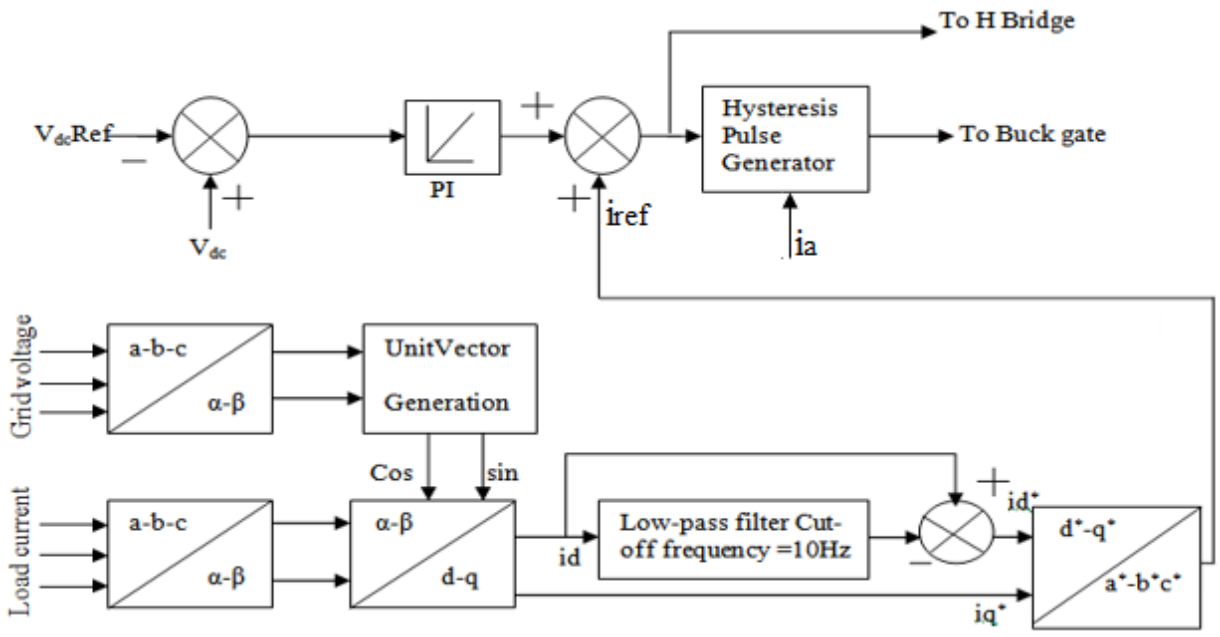

Figure 5.6 Complete control scheme

The main duty of the dc-bus condenser is to act as fixed dc storage for the converter to generate the feeding current to the grid current. The reference dc-bus $V_{dc\text{-}ref}$ voltage is compared with the measured dc bus voltage V_{dc}. The error is given to the PI regulator to cancel steady state errors. The output of the PI controller is added to the current reference signal to speed up the dynamic response and this current is directly used to switch H-bridge. These reference signals are compared to the inverter currents for the generation of necessary switching pulses using hysteresis pulse generator.

5.6 Simulation and simulation results

To validate the proposed topology and effectiveness of the control scheme, simulink model of the ILI based DSTATCOM is developed and simulation analysis is performed using MATLAB/ Simulink block set. This model is tested for different power quality compensation constraints. To prove that the ability of the buck based inverter to perform as a controllable current source, a feedback control employing fixed band hysteresis current controller is used. A 3-phase, 3-wire distribution network is considered here and MOSFETs are selected as the semiconductor switches for the simulation study.

Table 5.1 Simulation parameters

PARAMETERS	VALUES
Buck inductance	10 mH
Buck capacitance	.4μF
Coupling inductance	6.5 mH
P	800 W to 3.5 kW
Q	600 VAR to 2.5 kVAR
Dc-link voltage	360 V
Dc-link capacitor	2000μF

5.6.1 Reactive power compensation by ILI-DSTATCOM

For verifying the ability of this system to compensate for reactive power, RL load of P= 800W Q=600 VAR is considered and the DSTATCOM is connected to the PoC at 0.1 seconds through a breaker. Simulation analyses are given in figure 5.7.

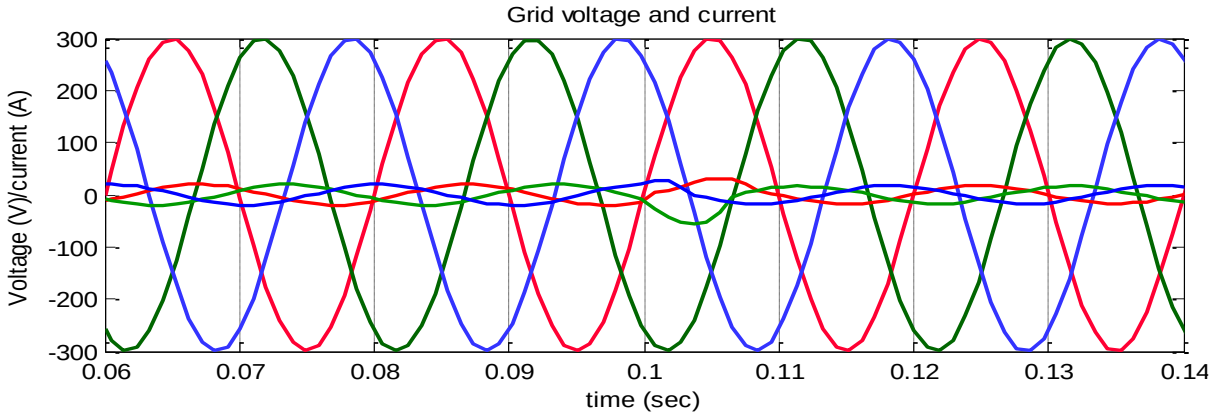

Figure 5.7 (a) Three-phase source voltages and currents (before and after compensation)

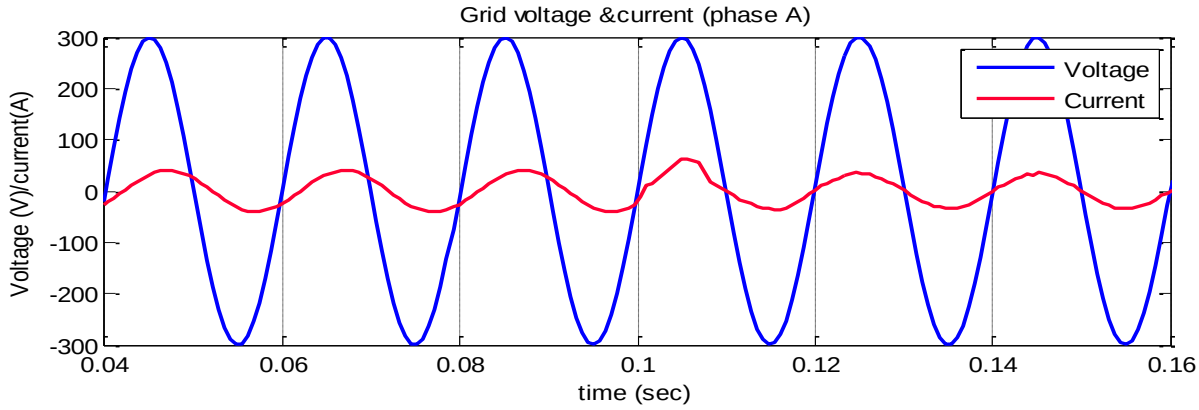

Figure 5.7 (b) Phase A source voltage and current (before and after compensation)

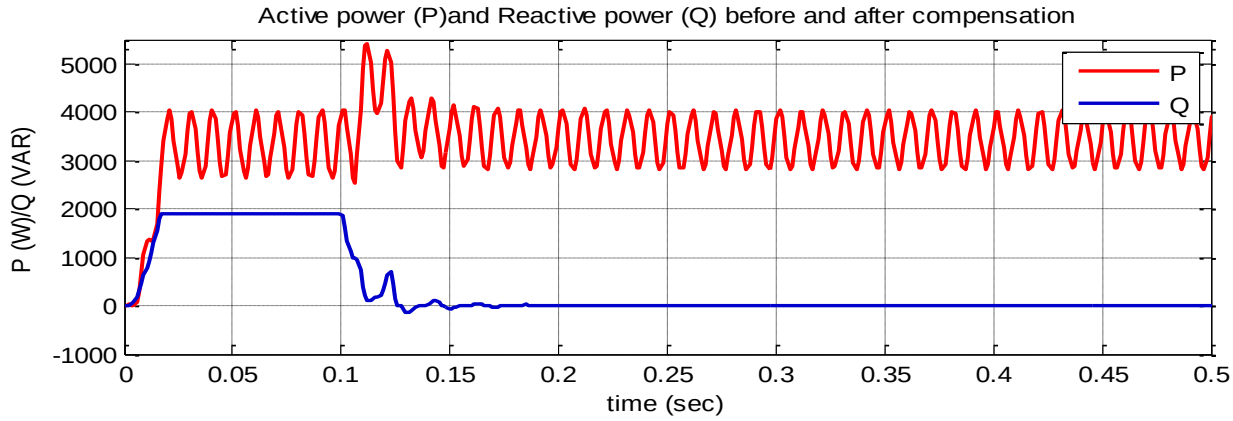

Figure 5.7 (c) Active and reactive power (before and after compensation)

Figure 5.7 (a) shows the three-phase grid voltages and currents. In this, the grid currents lag the grid voltages by certain angle that is clearly shown in figure 5.7 (b). After connecting the DSTATCOM, these current became in-phase with the grid voltage. Hence the ILI-DSTATCOM proved its ability to provide reactive power compensation. Figure 5.7 (c) shows the real and imaginary power delivered by the grid for before and after compensation. On connecting the DSTATCOM into the system, the entire imaginary power demand by the load is supplied by the DSTATCOM and hence the reactive power delivered from the source became zero after compensation and prior to the DSTATCOM connection to the grid, the imaginary power demand of the system was 2000 Var.

5.6.2 Harmonic filtering by ILI-DSTATCOM

A source with line-Line voltage of 415V is chosen and a three phase diode bridge rectifier with RL load with real load of "P" and reactive load of "Q" is considered as a harmonic load. The voltage applied across the dc bus is 360V. The dc-link voltage requirement of the ILI-DSTATCOM is lower than that of classical VSC. So that the voltage stress across the switching devices of this inverter is minimized to a larger extend. This ILI-DSTATCOM successfully tracked the current reference generated by SRF strategy. The source voltages and currents are given in figure 5.8 (a, b & c). These are purely sine wave and in phase after compensation. Figures 5.8 (d & e) show the inverter current and dc-link voltage respectively. Here the dc-bus voltage required for the compensation is very less. The source current shown in the figures are scaled up by 5.

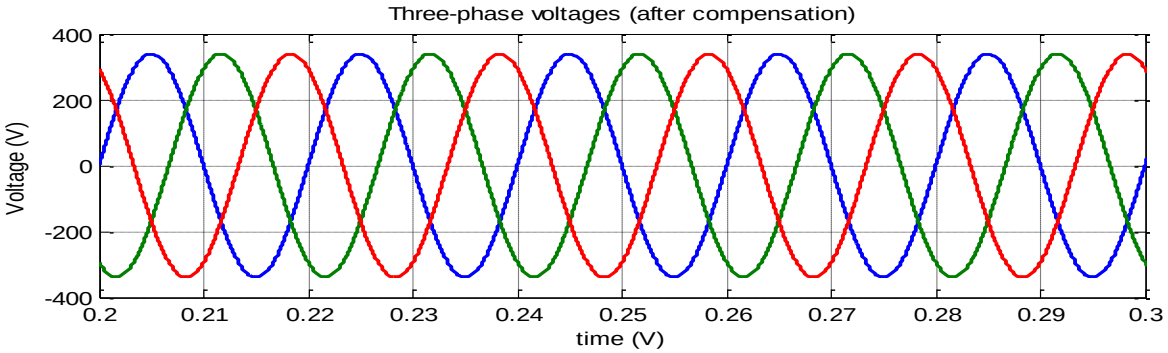

Figure 5.8 (a) Three-phase voltages after compensation

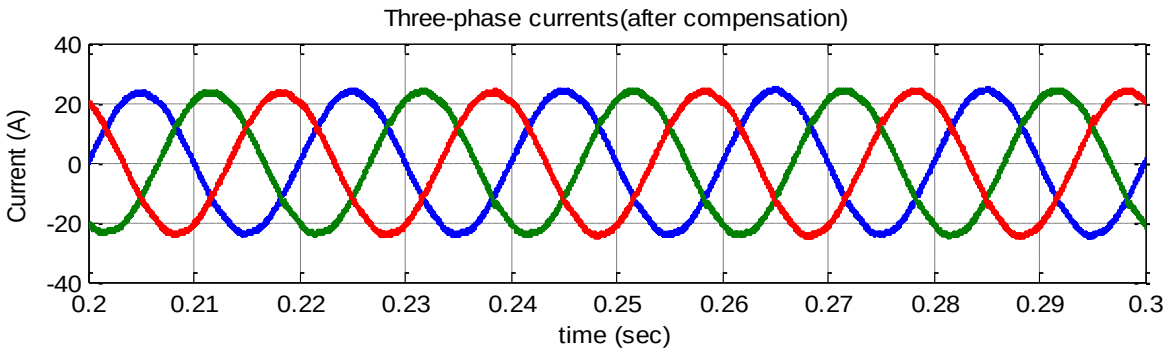

Figure 5.8 (b) Three-phase currents after compensation

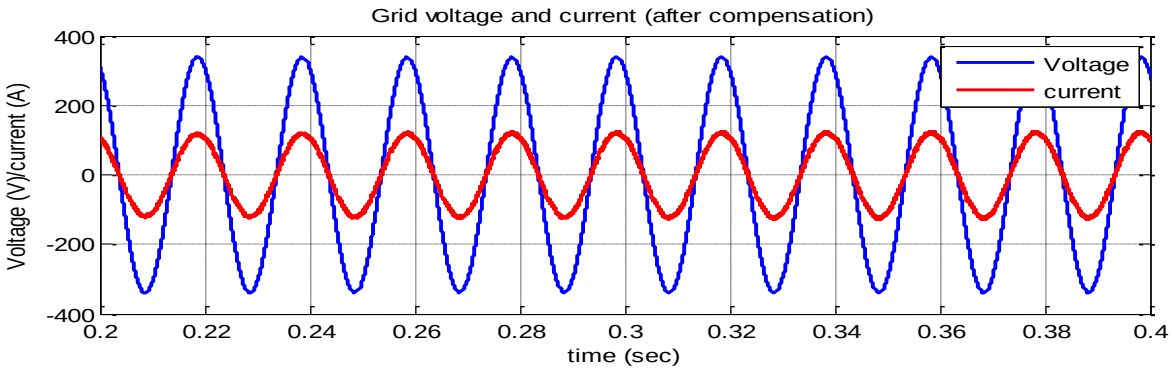

Figure 5.8 (c) Single-phase voltage and current after compensation

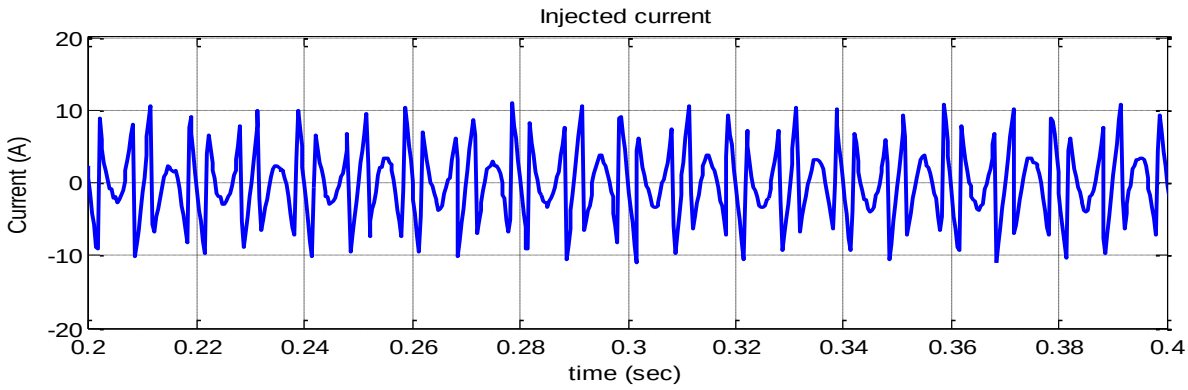

Figure 5.8 (d) Injected current

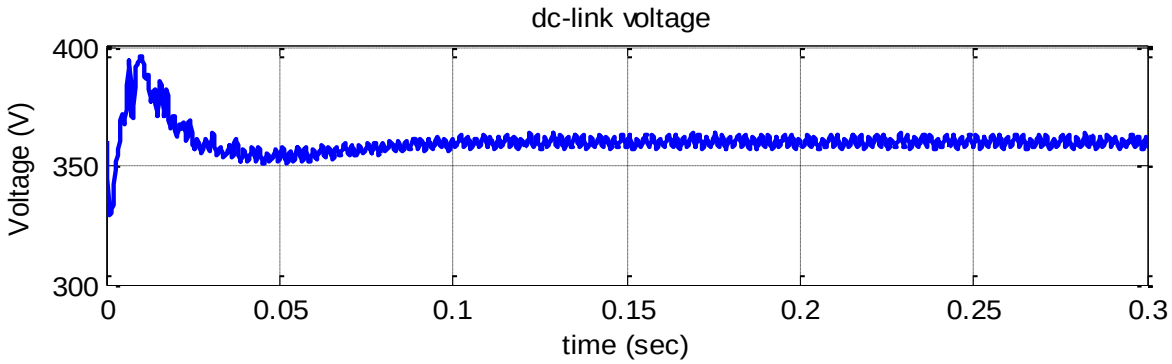

Figure 5.8 (e) Dc-link voltage

In order to observe the dynamic characteristics of the DSTATCOM, consider the condition that the DSTATCOM is not connected into the network in the beginning. The ILI based DSTATCOM system is applied to the grid at 0.1 seconds, within 0.025 seconds current waveform became steady as shown in figure 5.9 (a). Before and after compensation voltage and current for single phase is given in figure 5.9 (b).

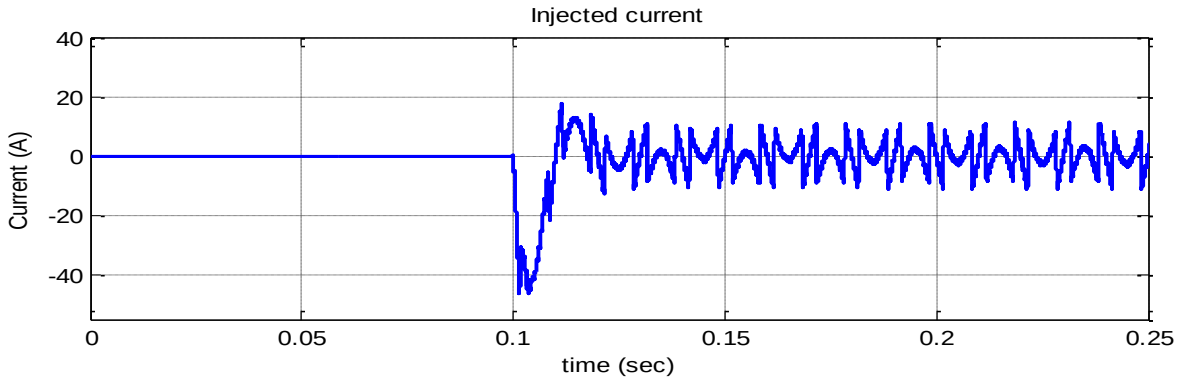

Figure 5.9 (a) Injected current before and after compensation

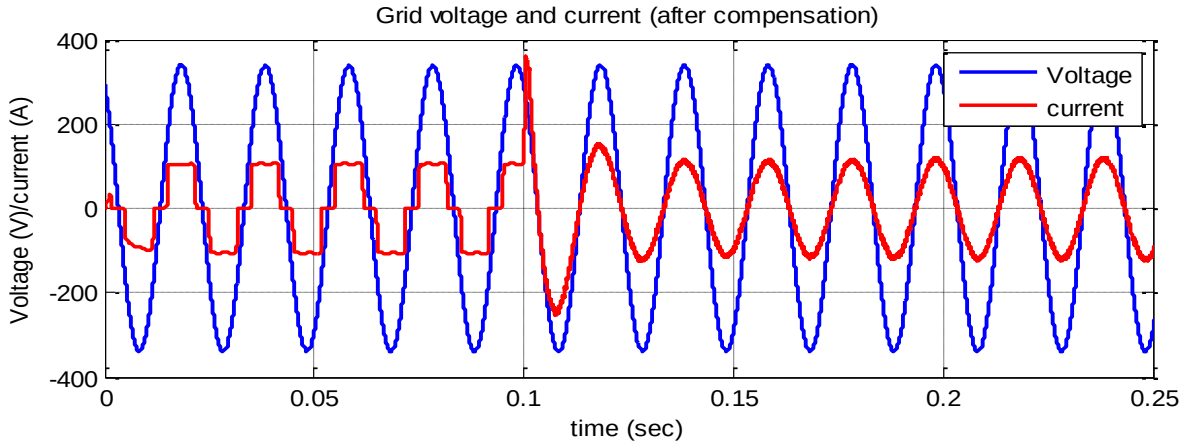

Figure 5.9 (b) Source voltage and current before and after compensation

Figure 5.10 shows the capability of the ILI based DSTATCOM to supply for the dynamic changes in nonlinear load. The non-linear load is increased suddenly at 0.5 seconds. The inverter showed excellent performance towards this change and without any transients it followed the load increased. In figure 5.10 (a), (b), and (c) show the inverter injected current, the grid voltage and current for one phase and the real and imaginary power requirement correspond to the load

changes respectively. It is shown that the imaginary power requirement is zero even for rapid changes in the non-linear load.

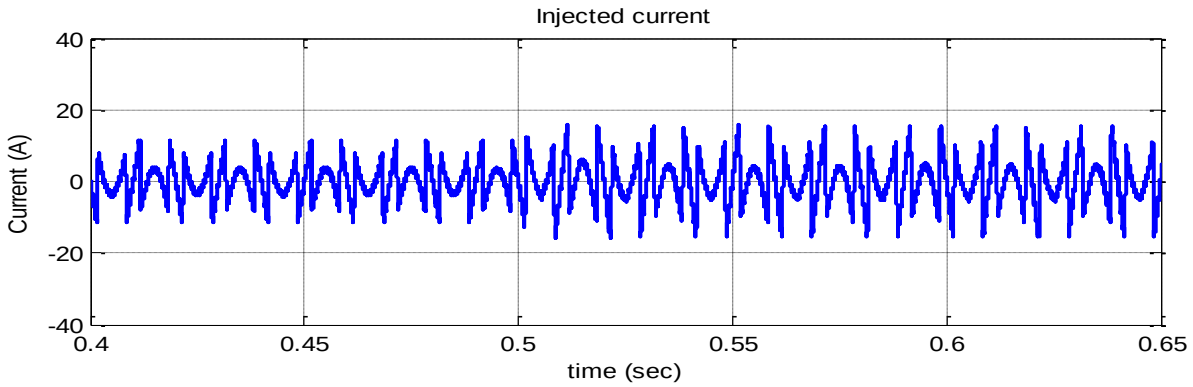

Figure 5.10 (a) Inverter injected current (sudden changes in the load)

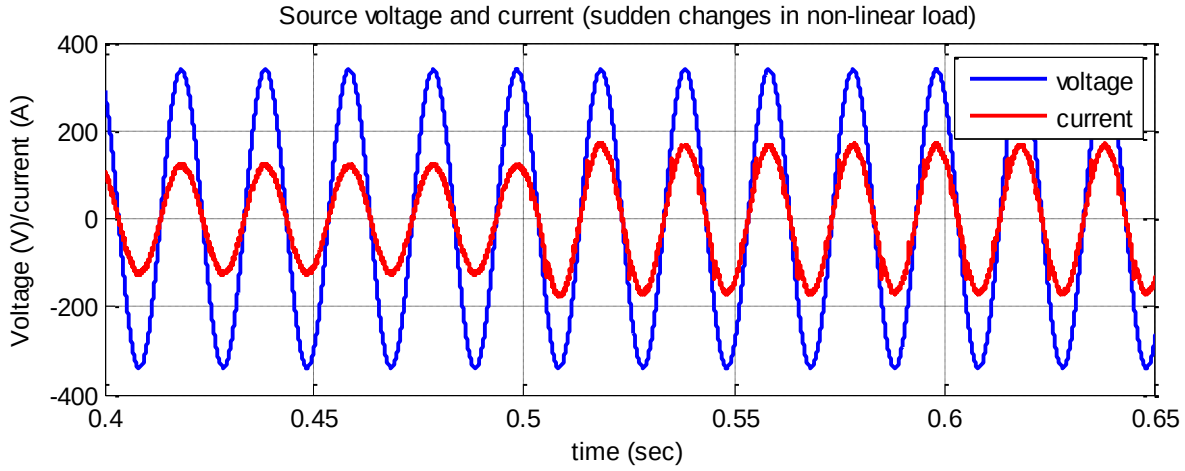

Figure 5.10 (b) Source voltage and current of phase A

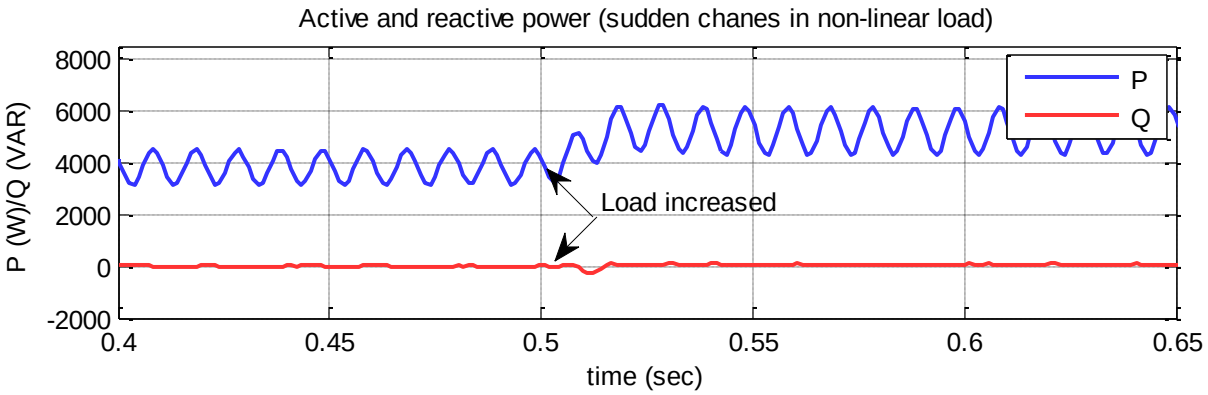

Figure 5.10 (c) Real and reactive power for load changes

The FFT analysis of ILI based DSTATCOM is shown in figure 5.11 when it is being subjected to harmonic current elimination and reactive power compensation. THD of grid voltage is 0 % and THD of the source current is 1.77 %. In this system, the THD is very low when compared to VSI topology. So in a nutshell, ILI based inverter characteristic shows superior performance when subjected to DSTATCOM application. Moreover, the harmonic content in line voltage of the ILI is minimized as it is more sinusoidal than 2-level VSI.

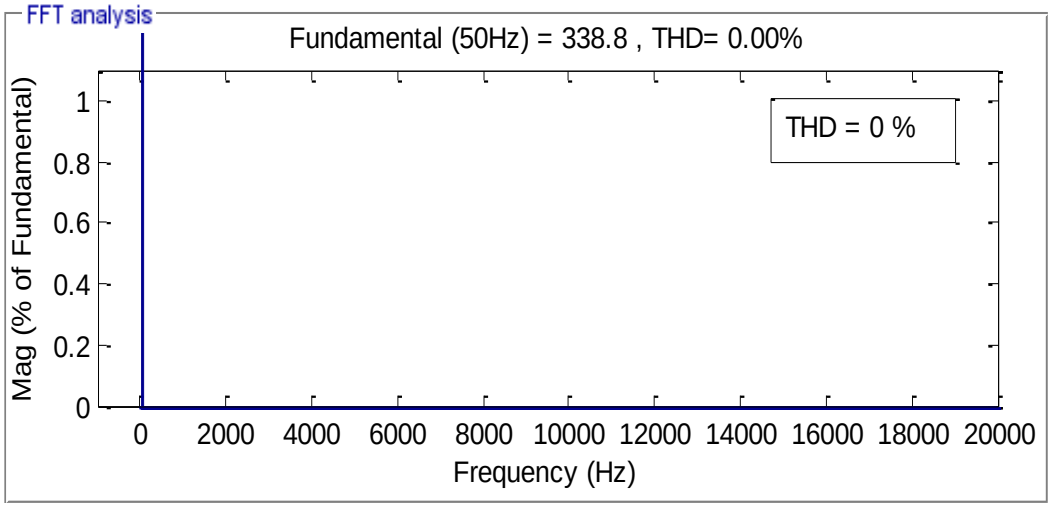

Figure 5.11(a) FFT analysis of source voltage (THD = 0 %)

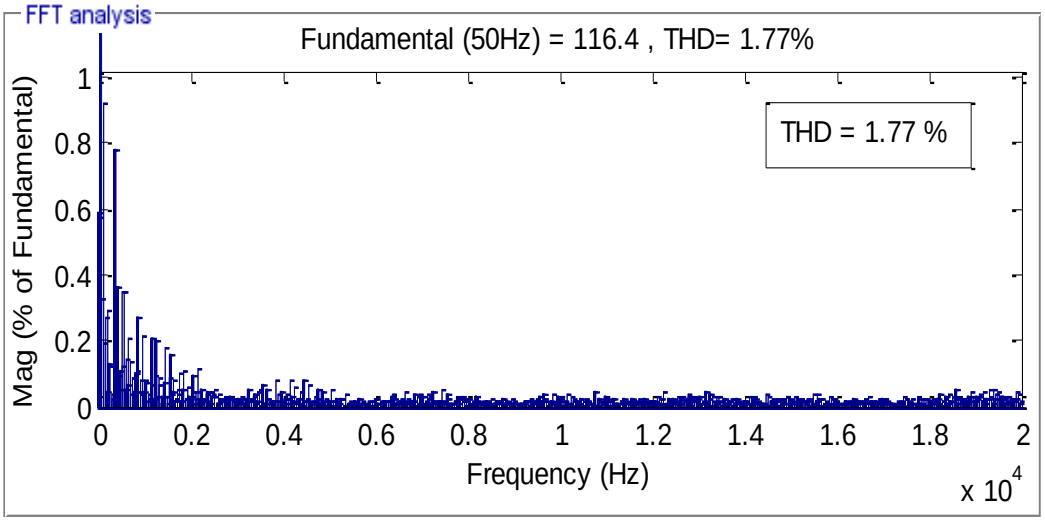

Figure 5.11(b) FFT analysis of source current (THD = 1.77 %)

5.7 Comparison with traditional VSI

For the operation of conventional DSTATCOM in the linear PWM region, the dc-link voltage of the DSTATCOM should be kept at a voltage higher than the maximum value of PCC line voltage. The dc-bus voltage needed for the ILI to produce the three-phase sinusoidal voltage is very low as compared to the conventional VSI. For instance, in traditional VSI, for the successful performance of DSTATCOM, the voltage across the capacitor must be at least 150% of the maximum line-line supply voltage. So the switching devices in 2-level VSI are suffered to severe voltage stress of 680V. On the other hand, in this topology, the capacitor voltage requirement is just 360V to obtain AC voltage with maximum amplitude of 630V and rms value of 440V. Therefore, the dc-bus utilization is higher and the voltage stresses across the switching devices are reduced. The higher dc-link voltage increases the rating of the system that leads to high cost, size, and weight of the system. Additionally, the dc-link capacitor increases the initial and running costs of the system and also drives up the control complexity. In this ILI based DSTATCOM, dc capacitor can be used as a dc-link capacitor and hence can reduce the cost. This topology also avoids the use of line frequency transformer thereby reducing cost, weight, volume and size of the system.

5.8 Summary

While designing a DSTATCOM circuit, mitigation of harmonics in the feeding current, reduced THD and minimized voltage stresses are the prime factors to be considered. In this chapter, an ILI based DSTATCOM is suggested. This topology avoids extra filter circuit to gain the goal. The simulink model of this compensator is developed and various performance analyses are conducted considering various operating constraints. The reactive power compensation and harmonic elimination demonstrate the better reliability of the proposed system. It also exhibits excellent dynamic performance. It has excellent capability to track reference current and the grid voltage and current are exactly in phase. The injected current harmonics is very low. It is an excellent remedy for harmonic elimination and reactive power compensation because of its outstanding performance, highest dc-bus utilization and minimized voltage stress. It consists of only one switch in each phase operating at high frequency so that the switching power losses of this converter is minimized to a great extent and has a benefit of absence of shoot-through

menace. Its excellent steady state and dynamic performances of this DSTATCOM outweigh other inverter topologies for the same field of application. An experimental set up is developed to justify the simulation results that closely match to the simulation results which would be discussed in the chapter 7. The behavioral study is carried out for different operating conditions. This topology avoids the use of additional filters and decreases the rating of the dc-link voltage capacitor. With good reference tracking performance, this topology is suitable for industrial applications. The constant voltage operation of this DSTATCOM provides the ability to resist disturbances and can enhance the stability of the system.

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Chapter 6

PV DSTATCOM–ILI for reactive power control in PV supported distribution network

6.1. Introduction

Nowadays the idea of interfacing small and moderate-sized generation systems into electrical system is escalating worldwide. These generation units are popularly known as Distributed Generation (DG) units. The DG units act as an alternative electricity generating sources that can be directly connected to local load or connected to the electrical network by means of power electronic converters. The operating performance of such units does not affect the working of the electrical system so that their impact can be avoided. The grid connected DG inverters are attracting a lot of attention owing to the fact that traditional electrical energy networks are being subjected to more stresses due to demand of electricity, power delivery capability limits, difficulty in building new power lines and blackouts. The improvements in power electronic semiconductor devices and various digital control techniques are facilitating more feasibility and better flexibility to adopt these DG units in traditional electrical energy systems. This helps to enhance electrical energy generation and to improve the network stability through the power flow regulation.

Solar power generation is turned out to be one of the most significant sources of renewable energy. It is widely accepted that photovoltaic generations are presently alluring a lot of attentiveness to meet users' requirement in the distributed generation market. The stable and sudden growth of solar photovoltaic (PV) installation across the world has been steered by several aspects including renewable portfolio standards, reducing cost of installations and incentives such as feed-in-tariffs or net-metering mandated by authorities. The improving capacity addition of solar PV and installation of larger power plants has led to research and

development in high-power converter technologies for PV applications. The inter connection of solar photovoltaic (PV) units into the utility grid and enlarged amount of nonlinear loads lead to main power quality (PQ) problems such as current harmonics and high reactive power burden on the distribution network [112-116]. A new idea of utilizing PV solar farms as a compensating system is suggested in 2009 [117]. This concept called PVSTATCOM used the whole capacity of PV inverter during night time and the converter capacity remaining after active power generation during daytime to perform different grid support operations like voltage control, increasing the connectivity of adjacent wind farms [118], and improving the energy transmission capacity by power oscillations damping [119]-[120]. This concept is limited due to the fact that it cannot be applied when the solar system is producing its rated power output.

This chapter deals with the modeling and simulation analysis of grid connected solar photovoltaic (PV) based distributed generation system using ILI (chapter 4). It also analyzes the performance of this system as DSTATCOM (PV-DSTATCOM). This concept of utilizing PV solar system property can thus enhance power quality that would have otherwise needed costly extra components, like series/shunt capacitors or separate FACTS system controllers. To observe the ability of the PV-DSTATCOM for harmonics mitigation and reactive power compensation, the SRF strategy is used. The fixed band hysteresis current controller is used to follow the current reference extracted and the traditional PI regulator is used to control the dc-bus voltage. The simulation models are developed in the MATLAB/ Simulink and implemented in Sim Power Systems library. This chapter is organized as follow

Block diagram of the grid connected PV (GCPV) system is explained in section 6.2. Mathematical modelling of photovoltaic cell is briefed in section 6.3. Section 6.4 discussed the system description and Control of PV-DSTATCOM is explained in 6.5. simulation results are given in the section 6.6. Advantages of the system over traditional VSI is given in section 6.7 .and the chapter is concluded in section 6.8

6.2 Block diagram of the grid connected PV (GCPV) system

Grid connected PV system converts electrical energy into same magnitude, frequency and phase with the utility mains in addition to feeding the isolated loads. The block diagram demonstration of the GCPV system is shown in figure 6.1.

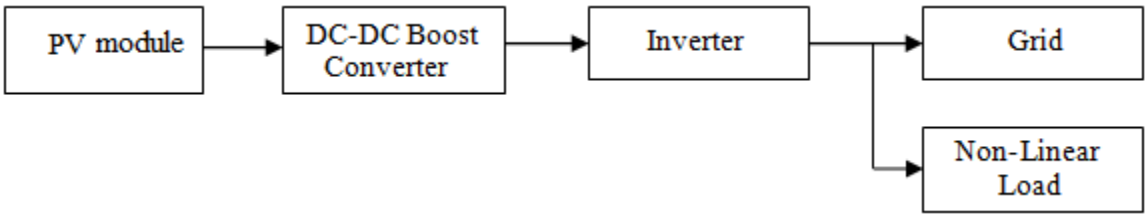

Figure 6.1 Block diagram of a two stage converter topology for GCPV system

It consists of a photovoltaic (PV) module that converts sunlight into electrical energy, a dc-dc boost converter to boost the dc voltage generated by the PV module and a dc-ac converter that converts the average output voltage of boost converter into an alternating quantity. The basic component of a PV system is the PV cell. These cells are connected in a different manner to make modules or arrays. The voltage and current available at the output terminal of the PV system can directly feed light loads such as lighting loads, dc motors and so on. More innovatory implementation requires power electronic inverters to process the electricity from the PV. These inverters can be used for various purposes such as regulating the voltage and current at the load, controlling the power flow in grid-connected systems and so on.

6.3. Mathematical modelling of photovoltaic cell

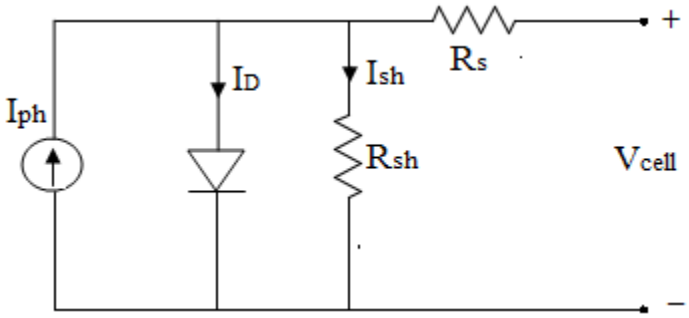

Figure 6.2 Single diode model of a photovoltaic cell

Figure 6.2 shows a basic circuit configuration of photovoltaic system. It is a single diode model that composed of a current source, a diode, a series resistance and a parallel resistance. The light generated current of the solar cell is indicated by the current source (I_{ph}), the diode represents the nonlinear impedance of the p-n junction and is connected in anti parallel with the current source, the series resistance (R_s) demonstrates the internal power losses and the shunt

resistance attributes to the leakage current to the ground. When solar radiation falls on the cell, the direct current is generated that has a linear relationship with solar radiation.

The module photo-current I_{ph} is given by the following equation and is depends on the solar irradiation and temperature.

$$I_{ph} = \left[I_{sc} + K_i(T - 298)\right] * \frac{I_r}{1000} \text{.....(6.1)}$$

Where I_{ph} represents the photo-current in ampere (A), I_{sc} is the short circuit current, K_i is the short-circuit current of cell at 25° C and 1000 W/m^2, T is the operating temperature in Kelvin (K), and I_r is the solar irradiation in W/m^2.

Mathematical expression for module reverse saturation current I_{rs} is:

$$I_{rs} = \frac{I_{sc}}{\left[\exp\left(\left(qV_{oc} \big/ N_s knT\right)\right) - 1\right]} \text{.....(6.2)}$$

Where, q is the electron charge, =1.6 *10^{-19} C, V_{oc} is the open circuit voltage in volts, N_s is the number of series connected cells, n is the diode ideality factor, and k is the Boltzmann's constant, = 1.3805 *10^{-23} J/K.

The module saturation current I_o varies with the cell temperature and is given by the equation:

$$I_o = I_{rs}\left[\frac{T}{T_r}\right]^3 \exp\left[\frac{q.E_{go}}{nk}\left(\frac{1}{T} - \frac{1}{T_r}\right)\right] \text{.....(6.3)}$$

Here, the nominal temperature T_r = 298.15 K, E_{go} is the band gap energy of the semiconductor, = 1.1 eV. The current output of PV module is:

$$I = N_p \times I_{ph} - N_p \times I_o \times \left[\exp\left(\frac{V \big/ N_s + I \times Rs \big/ N_p}{nV_T}\right) - 1\right] - I_{sh} \text{.....(6.4)}$$

where

$$V_t = \frac{K \times T}{q} \quad \text{.....(6.5)} \qquad \text{and}$$

$$I_{sh} = \frac{V^{N_p}\!/_{N_s} + IR_s}{R_{sh}} \quad \text{.....(6.6)}$$

where N_p is the number of parallel connected PV modules, R_s is the series resistance in ohm (Ω), R_{sh} is the parallel resistance, and V_t is the terminal voltage.

Here the PV module is modeled as a current source where the current generated by the solar cell is depends on the solar irradiation intensity falling on it and temperature. In order to achieve the desired power, more cells can be joined in cascaded and shunt fashion. The simulation of solar module is analyzed using MATLAB/ SIMULINK model based on the above mentioned equations.

6.4 System description

The PV module can be directly connected to the local loads via ILI. For grid connected applications of photovoltaic system, two converter stages namely a dc-dc boost converter and a dc-ac inverter (ILI) are used as shown in the block diagram (figure 6.1). The PV-DSTATCOM system architecture is shown in figure. 6.3. Here, the dc power produced by the solar PV module is given to the dc bus of the ILI and is joined at the point of connection in the distribution network that feeds a non-linear load. The basic operating principle of PV-DSTATCOM is similar to that of DSTATCOM that can produce and draw reactive power. The PV-DSTATCOM is capable of providing variable magnitude of shunt compensation continuously by injecting current into the distribution network. It mainly consists of an ILI and a dc-link capacitor.

The ILI consists of four fundamental frequency operated switches SI-S4 per phase, each consists of a power electronic switches and an anti-parallel diode. The power electronic switches can be either a power MOSFET for small power application or a gate turn-off (GTO) thyristor for large power application. However, for distribution network applications, the better choice is normally the insulated gate bipolar transistor (IGBT) as it can withstand fairly high current, speedy switching characteristics, and decreased losses. ILI injects compensating current at the point of common connection (PoC) through interfacing reactor. A PV-DSTATCOM works as a

current source that injects required amount of compensating current to compensate for current harmonics and reactive fundamental current demanded by the non-linear load. It also injects the required load real power from PV source to load. When there is no sunlight (during the cloudy for instance), the ILI only compensates for the reactive power demand of the load.

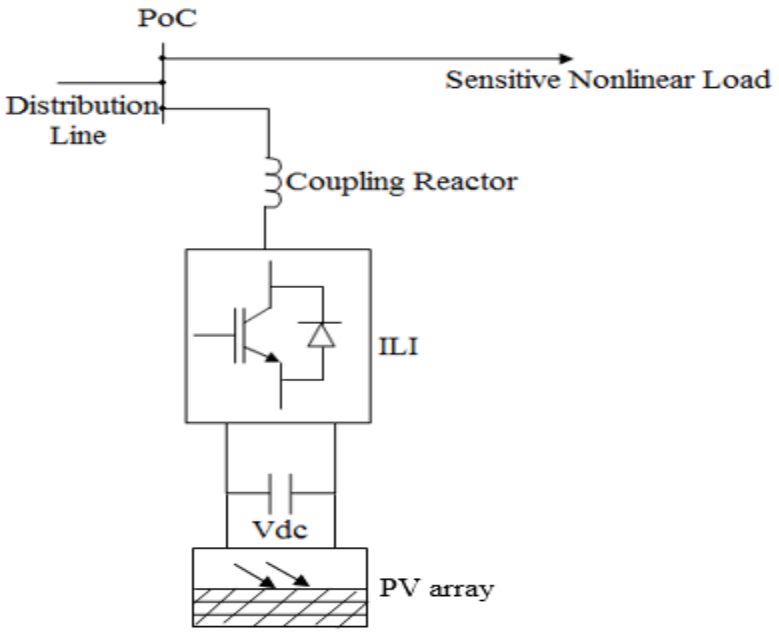

Figure 6.3 (a) Architecture of the PV-DSTATCOM

The application of photovoltaic system into the grid is done in two stages through infinite level inverter (ILI). In this case also the SRF strategy is utilized to extract the reference current that assures better utilization of the photovoltaic system. According to this algorithm, during the day this system feeds real power into the utility mains and at the same time compensates for the reactive power demand of the load. But active power exchange is out of the scope of this work.

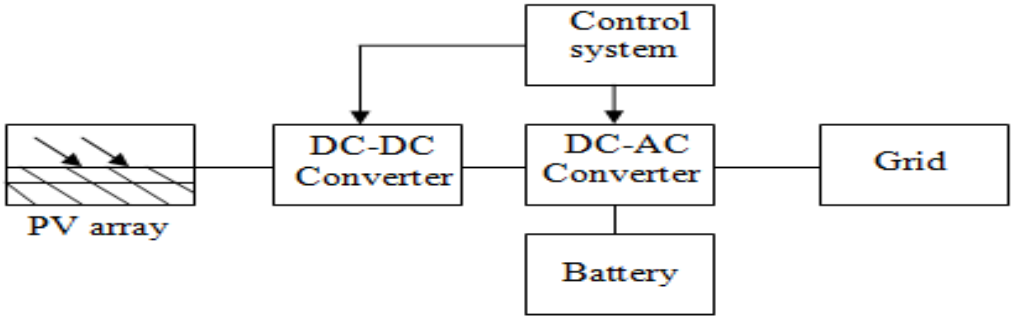

Figure 6.3 (b) Block diagram of the PV-DSTATCOM

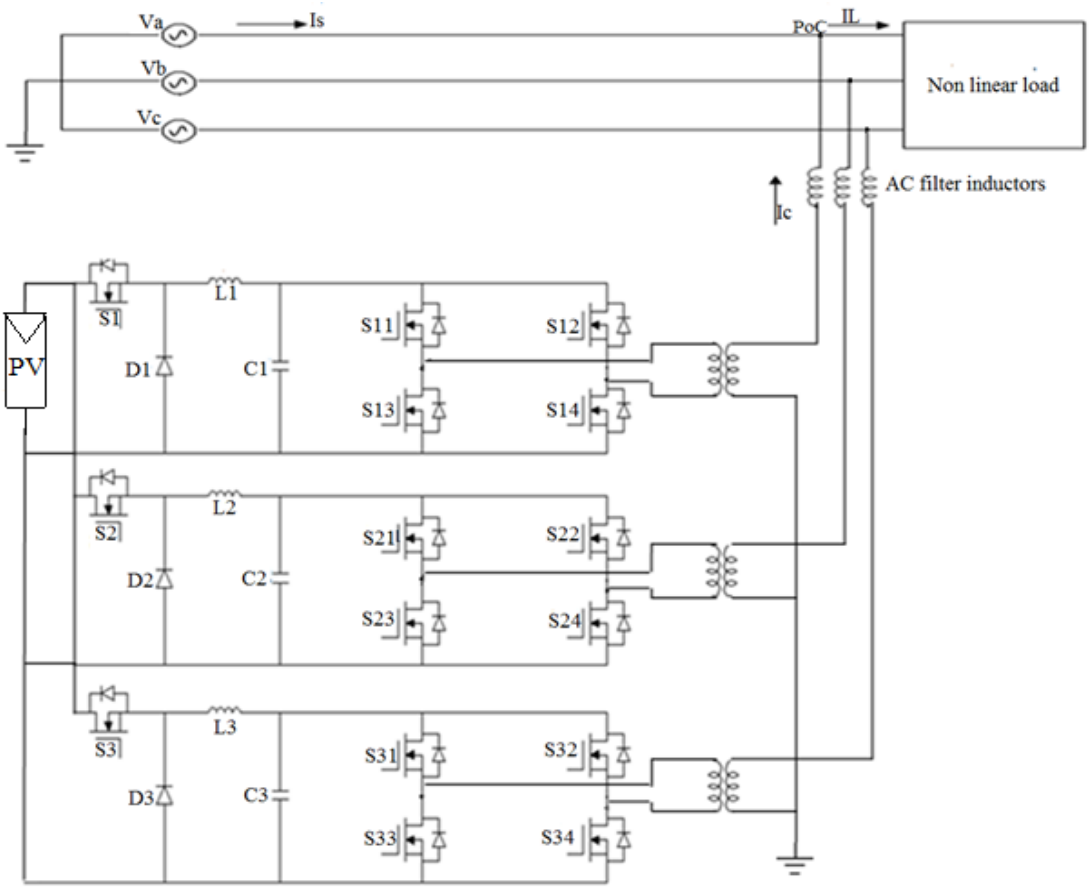

Figure 6.3 (c) Circuit diagram of the PV-DSTATCOM

6.5 Control of PV-DSTATCOM

Different inner control techniques are proposed in the open literature for the operation of PV-STATCOM, yet many control algorithms are not matured. However, the most widely accepted STATCOM control algorithms are being applied to PV-STATCOM applications. Recent researches utilized IRPT algorithm, d-q method, synchronous detection algorithm, IcosΦ algorithm and so on. This study utilizes a control algorithm based on the d-q (SRF) reference frame strategy (detailed in chapter 3). This strategy is simple to implement and it requires the use of PLL for the synchronization of the converter output with the grid. For harmonic current mitigation and reactive power compensation an appropriate controller is necessary for solar converter. These controllers composed of two control loops, the inner control loop for harmonics elimination and reactive power compensation in the network and the outer control loop to control dc-link voltage. Here, the active power from the PV panel is used to maintain dc-bus voltage of

the capacitor and to compensate for the losses in the converter. The voltage at the PoC is regulated by reactive power transfer between the PV converter and the utility mains. Hence, the actual measured dc-link voltage at the PoC is differentiated with the pre set value and the error signal is given to the PI controller to produce current reference. The PoC voltage regulator parameters are tuned by a logical hit-and-error technique to obtain the rapid step response, minimum settling time, and a peak overshoot of 10%–15%. The power factor (PF) control is known as one of the most significant problems in interfacing PV generators to the grid because they are normally working at unity PF. The Phase Locked Loop (PLL) circuit is utilized to synchronize the current reference generated with the utility voltage in the PV power conversion system. So the PLL is considered as a very significant section of the PV system control. The classical reactive power control regulates only the reactive power output of the converter such that it can perform unity power factor operation together with dc-link voltage regulation. Also there are two control algorithms: the open loop control method and the closed-loop control method for the current controller. Since the open loop control methods are easy to implement, it is widely implemented in numerous applications. However, it is sensitive to the parameters change. The closed loop control algorithms are capable of achieving better performance even in the presence of different noises. So, hysteresis current controller is utilized in this study to follow the reference current extracted by using SRF algorithm. To generate the proper switching pulses for the operation of the ILI, the d-q components of the modulating signal are transformed into three-phase sinusoidal modulating signals and compared with the actual current.

The control system used to control the PV-DSTATCOM is same as that used for ILI-DSTATCOM (chapter 5, figure 5.6). Here the PV-DSTATCOM detects the three-phase grid voltages and currents of non-linear load and generates command current signal. The current controller tracks the actual compensation currents and produce switching pulses for the operation of PV-DSTATCOM inverter. Here, as in case of DSTATCOM, out of three load current components (active, reactive and harmonic), only the active element is delivered from the grid to operate at unity power factor. The compensation circuit should then inject the remaining part to the ac network. The D-STATCOM control systems exert voltage regulation where an error signal is attained by comparing the reference signal with measured signal at the load point. The PI regulator processes the error signal and produces the required delay angle δ to switch the error to

zero, i.e., the load rms voltage is brought back to the reference voltage. The output signal from the PI regulator is added to the reference signal in d-q frame to produce the switching pulses for the ILI gates.

6.6 Advantages of the system over traditional VSI

This system avoids the use of line frequency transformer that used with VSI topology thereby reducing the cost, weight, size, and volume of the complete system. It does not require any additional filters to maintain power quality standards while the conventional VSI topology uses large LCL or L filter in the front end. It provides stable operation for change in solar insolation and cell temperature and increased reliability. Better utilization of dc bus voltage decreases the voltage stress across the switches. The VSI based system requires high dc-link voltage to ensure satisfactory operation thereby resulting high voltage stresses across the switches. It also contributes to high cost, size, weight, and rating of the system.

6.7 Simulation Results

To verify the effectiveness of the PV-DSTATCOM circuit to compensate for various power quality improvements, the entire circuit is simulated in Matlab / Simulink environment with a non-linear load of three-phase diode bridge rectifier along with RL load. Since the main goal of this chapter is to enhance power quality, MPPT controllers for the PV has not been considered. The PV-DSTATCOM circuit consists of a single diode type equivalent circuit of PV cell, a switched mode boost converter stage and the ILI circuit. The output of the current source is directly proportional to the solar power. The voltage from the PV panel is fed to the boost converter to increase the voltage magnitude and then given to the three-phase distribution grid of 50 Hz and phase to phase rms voltage of 400 volts through ILI and a coupling reactor. The output real power produced from the PV panel is used to compensate for the power losses in the dc-link. The fixed band of hysteresis current controller is 0.5. Simulation parameters used for the simulation of PV-DSTATCOM is shown in table 6.1.

Table 6.1 Simulation variables

VARIABLES	VALUES
Buck inductance	10 mH
Buck capacitance	.4μF
Coupling inductance	6.5 mH
P	800 W to 3.5 kW
Q	600 VAR to 2.5 kVAR
Dc-link voltage	360 V
Dc-link capacitor	2000μF
Boost inductance	0.01 H
Boost capacitance	470 μF
Solar irradiation	1000 W/m^2
Operating Temperature	273 K
Open circuit voltage	104.5 volts
Short circuit current	11.36 amperes
Number of cells connected in cascaded	2
Number of cells connected in shunt	2

Results of the simulation analysis are shown in figures 6.4, 6.5 and 6.6. The PV and IV characteristics of solar PV are shown in figure 6.4. The PV output power is 1100 watts and the open circuit voltage and short circuit current are 104.5 volts and 11.36 amperes respectively. In the figure 6.5 (a), load current waveform for three-phase bridge diode rectifier and RL load is shown and the PV-DSTATCOM injected current is shown in figure 6.5 (b). Figure 6.5 (c) and 6.5 (d) show the three-phase source voltages and currents after compensation and that of one phase respectively. From these figures it is evident that the grid current is exactly in-phase with source voltage. So, it is proved that ILI is also able to provide necessary compensation for the PV supported distribution network. Figure 6.6 gives the nature of dc-bus voltage of the PV-DSTATCOM. In this case also ILI requires lower dc-link voltage (360 V) for the satisfactory operation of reactive power compensation and harmonic filtering.

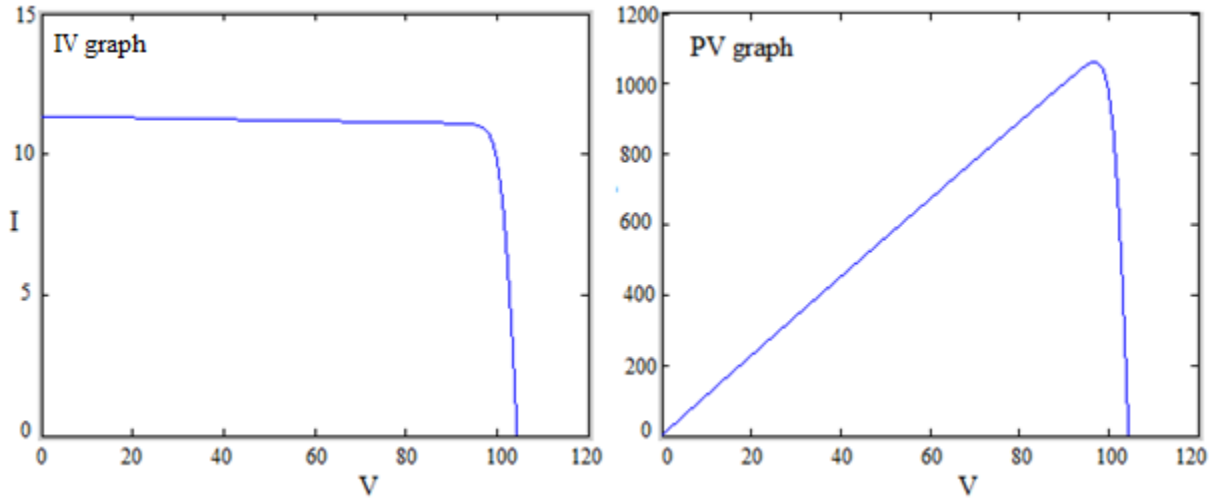

Figure 6.4 IV and PV characteristics of solar PV

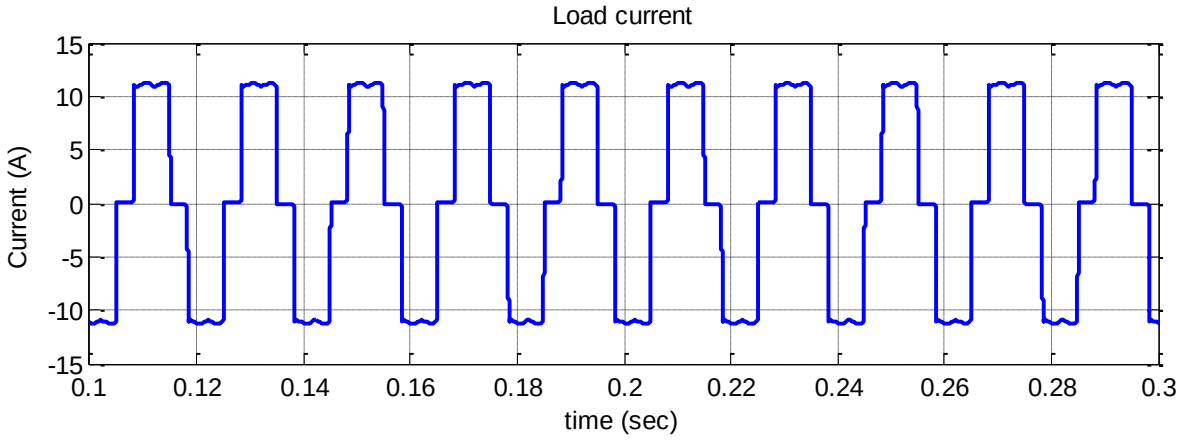

Figure 6.5 (a) load current waveform

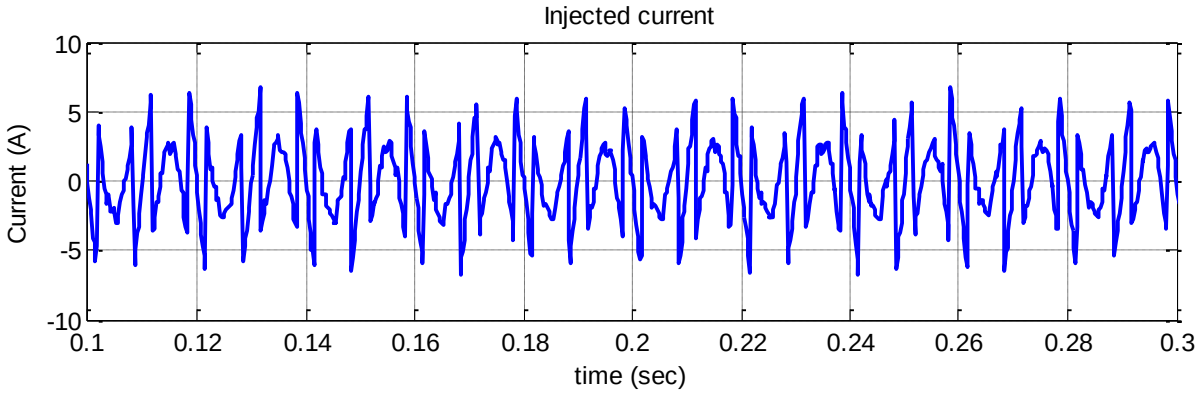

Figure 6.5 (b) PV-DSTATCOM injected current

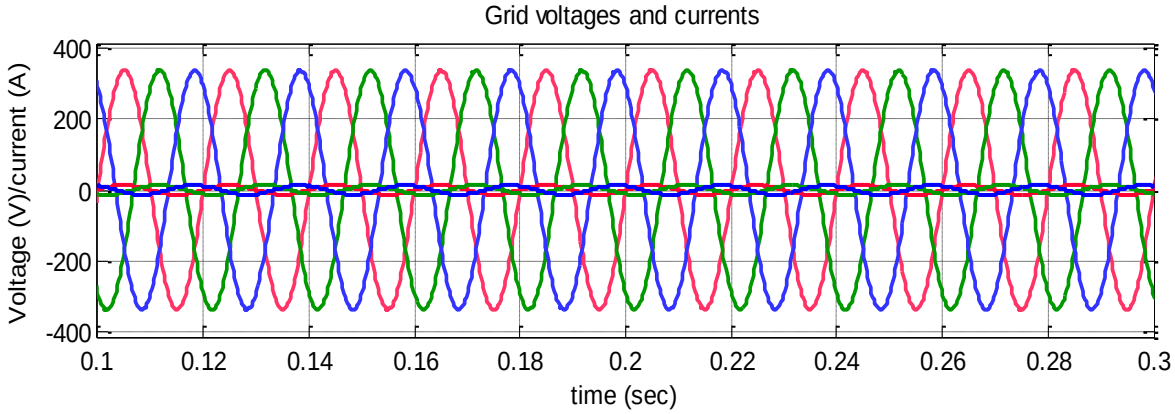

Figure 6.5 (c) Three-phase grid voltages and currents after compensation

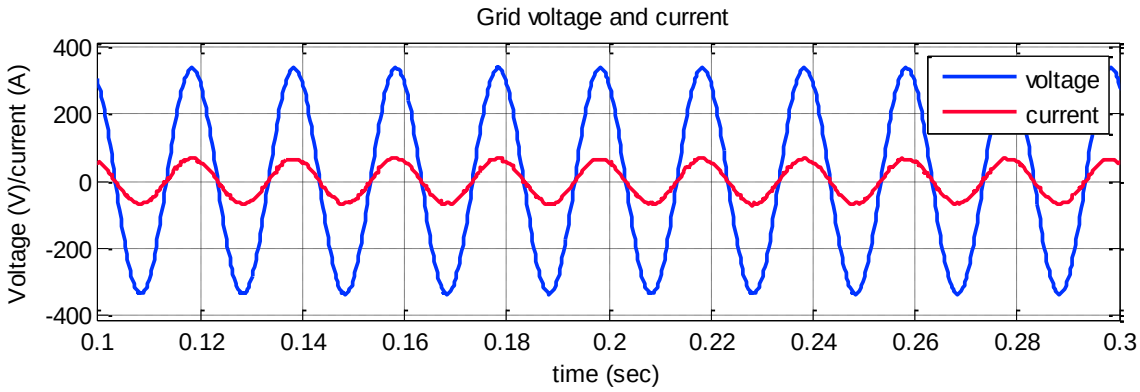

Figure 6.5 (d) Source voltage and current after compensation (one phase respectively)

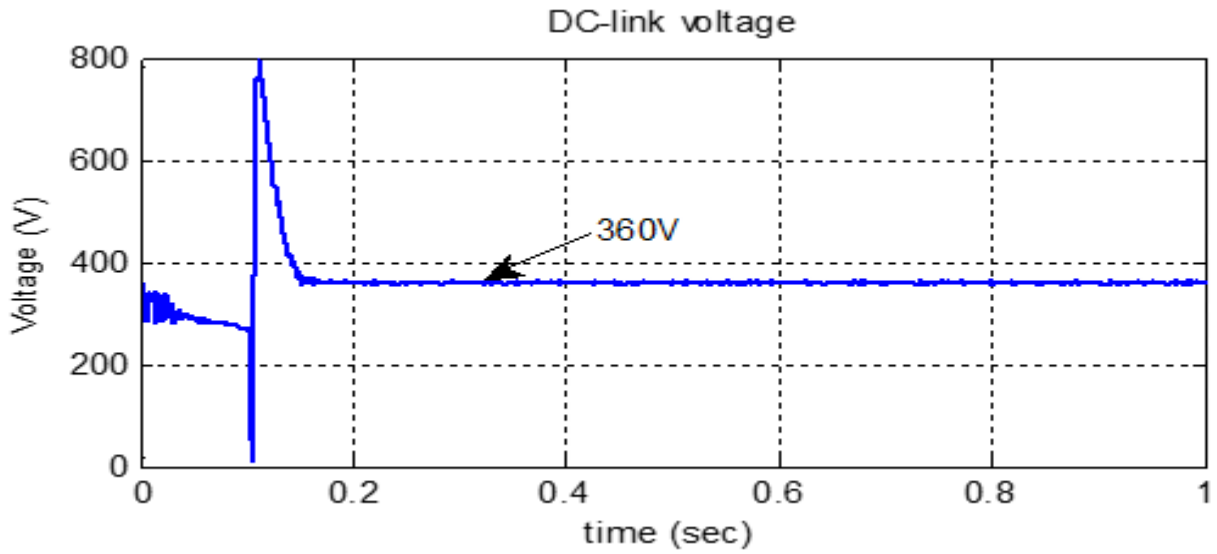

Figure 6.6 dc-link voltage of the PV-DSTATCOM

FFT analysis of the PV-DSTATCOM is shown in figure 6.7. Here, the total harmonic distortion of source voltage and current are 0.38 % and 3.0 % respectively. These are within acceptable limits. Hence the output waveforms are quality sine wave.

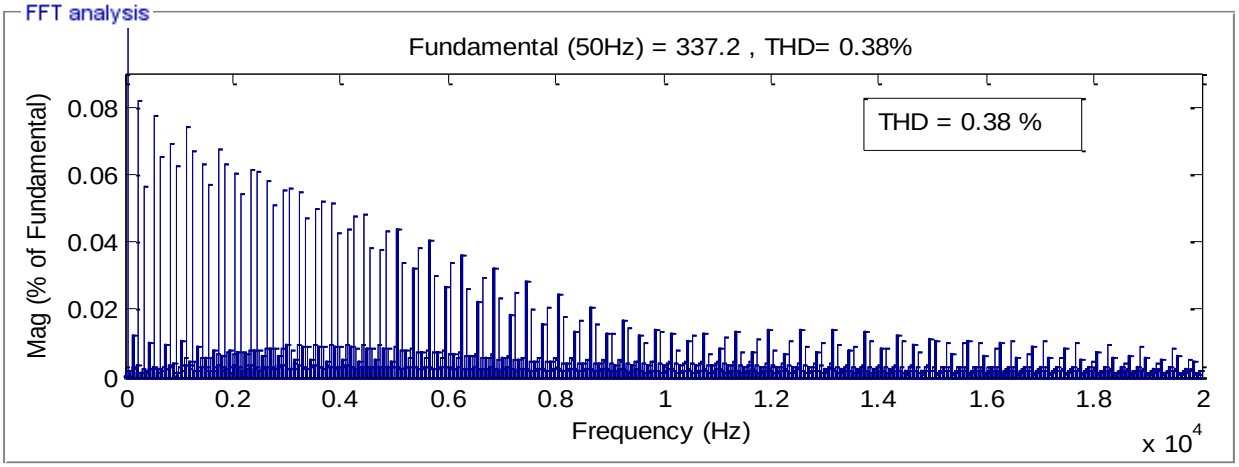

Figure 6.7 (a) THD of source voltage

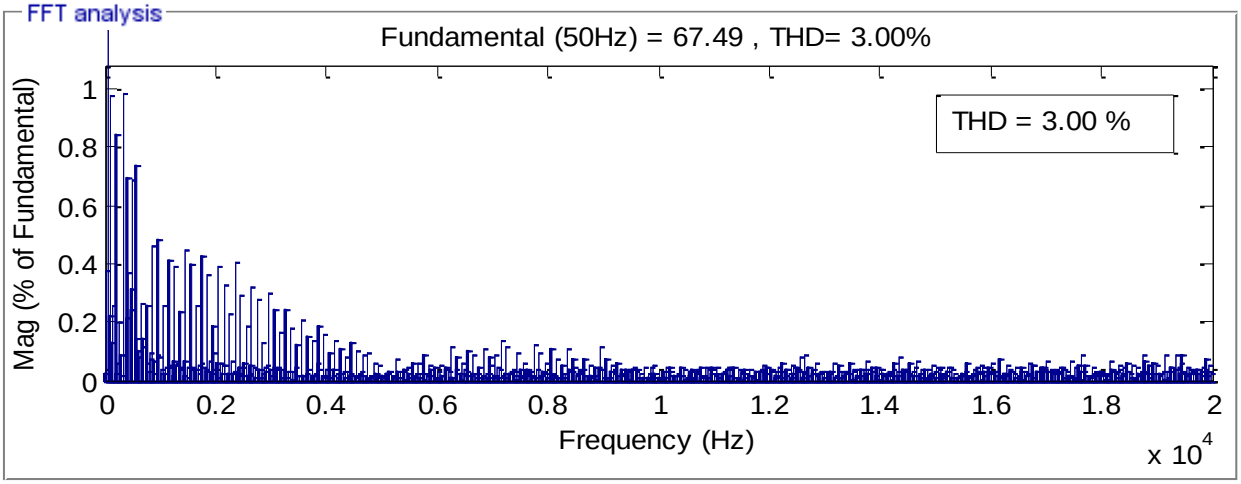

Figure 6.7 (b) THD of source current

6.8 Summary

Solar PV systems are idle during nights. So, it can be utilized to operate as a DSTATCOM with full capacity of interfacing inverter and during the day with remaining inverter capacity after active power production. A two staged PV-DSTATCOM is discussed in this chapter. A dc-dc boost converter is used in the first stage to boost the output from the PV panel to the sufficient level as the grid. This study utilized the ILI to connect the solar PV unit to the distribution

network and to compensate for the reactive and harmonic currents required by non-linear load with the presence of PV in the distribution network. A control technique based on SRF strategy has been used to control the PV-DSTATCOM. The use of SRF strategy to compensate for the imaginary power and harmonic filtering of the load is observed. The benefit of this control strategy is that the photovoltaic system is operated the whole day. In addition to this, the SRF strategy is simple to implement and it require the use of PLL to synchronize the inverter with the grid. The power quality enhancement performance of the PV-DSTATCOM is found satisfactory. The FFT analysis shows the THD is within the limit. It also has all the advantages of ILI such as reduced THD, minimized power losses and good response. Its greater dc-bus utilization decreases the voltage stress across the switches. The simulation results prove that the PV-DSTATCOM is very successful in obtaining high quality output waveform with lower THD.

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Chapter 7

Hardware Implementation of ILI based DSTATCOM

7.1. Introduction

National instrument's low cost multifunctional analog to digital data acquisition cards are widely used for the hardware implementation in the laboratories due to their accurate and superior performance. Data acquisition (DAQ) system observes an electrical or physical quantities using computer. It composed of sensors, DAQ observer, and a system with programmable software. DAQ unit acts as an interface between a computer and signals to be measured. It is one of the most important and efficient hardware solutions to implement control algorithms for power electronic inverters. The main features of this DAQ are high end parallel processing capabilities, reconfigurable hardware, high computational speed and low cost. This chapter discusses the hardware implementation and experimental results of the ILI based DSTATCOM using National Instrument's NI-PCIe 6351 data acquisition (DAQ) equipment and SCB-68A connector device. The control algorithm is implemented using Simulink Real time window. This chapter is organized as follow

Components used for hardware implementation is given in section 7.2. Hardware design is given in section in section 7.3 followed by hardware description in section 7.4. The experimental results are briefed in section 7.5. The chapter is concluded in section 7.6.

7.2 Components used for hardware implementation

1. ILI Circuit Board: It is designed for implementing the three-phase buck circuit of three-phase ILI. It is made of a rewirable arrangement comprising of 15A terminals and 1.5 mm^2 insulated copper PVC wire which can handle currents up to 15A. The whole circuit board is designed on

an acrylic board raised on a platform. Being rewirable, the same board can be used for all experiments conducted as a part of ILI topology.

2. Three Phase Inverter Stack: SKM50GB12T4, Fast IGBT4 Modules are used as switches. Three separate IGBT stacks are used to implement each phase of the three-phase ILI. Figure.7.1 a, b shows the SEMITRANS® 4 IGBT module.

Figure 7.1(a) SEMITRANS® 4 Fast IGBT module

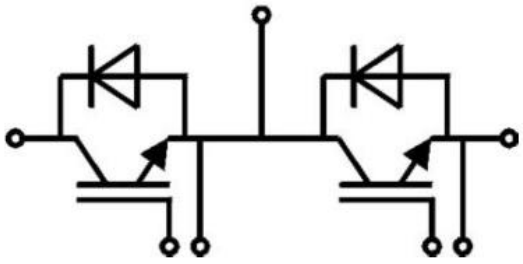

Figure 7.1(b) SEMITRANS® 4 Fast IGBT diagram

3. National Instruments PCIe-6351 Multi-function I/O device and Data Acquisition (DAQ) card with NI DAQ Device Custom Cable

Figure.7.2 PCIe-6351 Multi-function I/O device and Data Acquisition (DAQ) card and connector cable and connector block

4. 68-Pin Shielded Connector Block: The SCB-68A, shown in figure 7.3, is a shielded I/O connector block with 68 screw terminals for easy signal connection to a National Instruments 68-pin or 100-pin DAQ device.

Figure 7.3 SCB-68A

5. Voltage Transducer LV 25-1000: used to measure AC, DC and pulsed voltages.

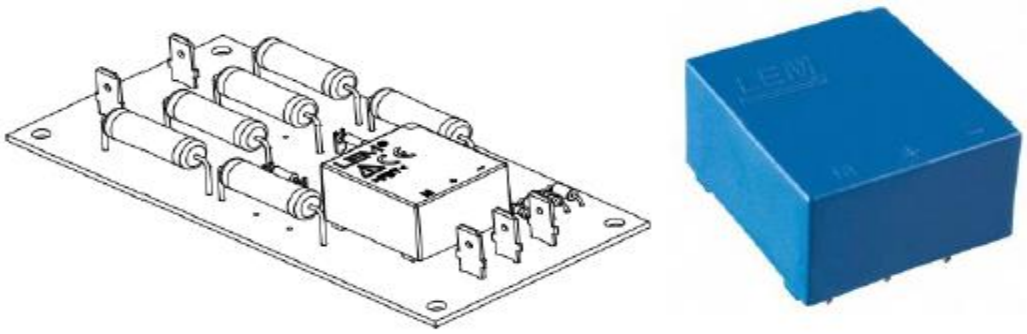

Figure 7.4 LV 25-1000 sensor

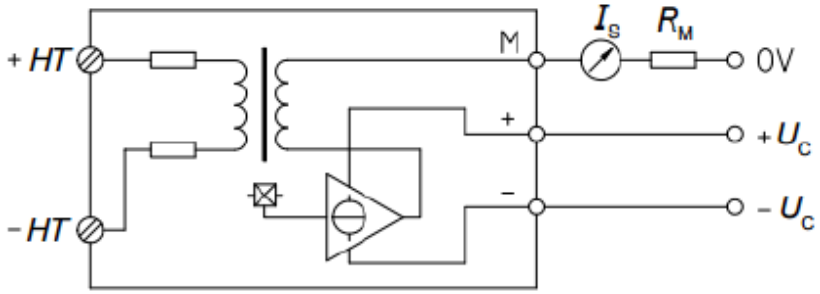

Figure 7.5 LV 25-1000 connection diagram

6. Current Transducer: LA 55 – P: used to measure AC, DC and pulsed currents.

Figure 7.6 (a) LA 55 – P

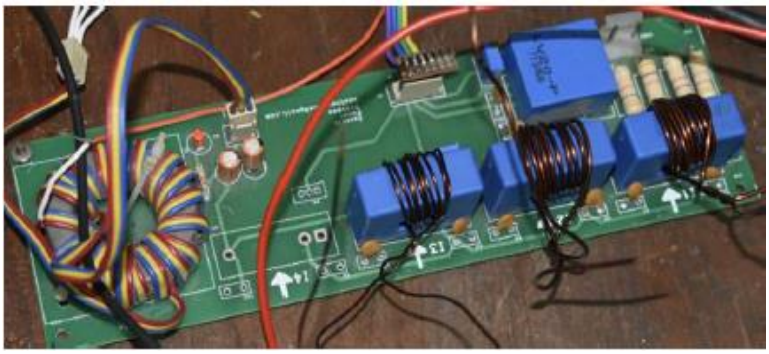

Figure 7.6 (b) LA 55 – P connection setup

7. Three-phase non-linear load: Three-phase bridge rectifier and a wire wound resistor of resistance 100 ohms is used as the non-linear load that has current carrying capacity of 50 A.

7.3 Hardware design

7.3.1 Design of high frequency buck circuit

1. SKM50GB12T4, Fast IGBT4 modules are used as HF switch. The PWM signal is provided at the gate through IGBT gate driver SKYPER32 R.

2. HF diode MUR 860 is used as the buck circuit freewheeling diode.

3. Inductor and Capacitor Design

The maximum load current I p = 2*2 A

Using SWG 20, number of turns is found by

$N=L$ I$p/BmAc$

Where, the flux density of ferrite core (Bm) = 0.2 Tesla

Ferrite core used is E 65/27 and core area Ac = 540 mm^2

N = (0.01×2) / (0.2×540×10^{-6}) =185 $turns$

Air gap length, lg = μNIp / Bm

$lg = 4\pi\varepsilon^{-7}$×182×2 / 0.2 = 2.3 mm

The general equation for voltage across inductance is given by $V = L\frac{dI}{dt}$

During the ON time $V_{in} = L\frac{\Delta I}{D/f}$

Where $V_{in,}$ ΔI, D and f are input dc voltage, ripple current, duty ratio and switching frequency respectively. Ripple current is taken as 30 percent of maximum load current. The value of inductance is given by

$$L = \frac{V_{in}D}{\Delta I * f} = \frac{325 * 0.4}{1.2 * 10 * 10^3} = 10.833 * 10^{-3} H$$

An inductor with above specifications was wound and was tested to give the required inductance of 10 mH. Three 10 mH inductors is designed for three-phase ILI and are designed as per above parameters with ferrite E65/27 core and 20 SWG copper wire.

The equation for buck capacitance is given by $C = \frac{T\Delta I}{8\Delta V} = \frac{1.04*10^{-6}*0.6}{8*200*10^{-3}} = .33*10^{-6}F$

Table 7.1 Hardware Parameters

Parameters	**Values**
Input voltage	325 V
Output voltage	400V
Power rating	90 W
Switching frequency	10 kHz
Buck inductor (E core)	10 mH
Buck capacitor(electrolytic type)	0.33 µF
HF diode	MUR 860

The dc-bus capacitor plays a vital role in the power circuit as it has direct impact on the harmonic distraction of the output voltage produced by the D-STATCOM and the speed of response of the regulator. The undersized capacitor makes the response of the regulator faster. The dc bus voltage may contain excessive ripple and hence high levels of harmonic distortion in the output voltage. On the contrary, an oversized capacitor improves the output voltage waveform shape and lower the transient overshoots but at the cost of a stagnant controller's response. In addition to this, coupling transformer reactance and transformation ratio must be properly selected as per the requirement such as voltage regulation and power compensation.

7.4 Hardware description

To prove the validity of the theoretical analysis and simulation results of ILI based DSTATCOM, a laboratory prototype is developed. Different variables used for the implementation of hardware setup and its specifications are shown in table 7.1. It mainly consists of 3-phase ILI converter circuit, 3-phase non-linear load, control algorithms, DAQ, connector set. The control algorithm is realized via simulink real time windows target. The hardware

structure of the suggested system is shown in figure 7.7 below and figure.7.8 shows the photograph hardware setup implemented.

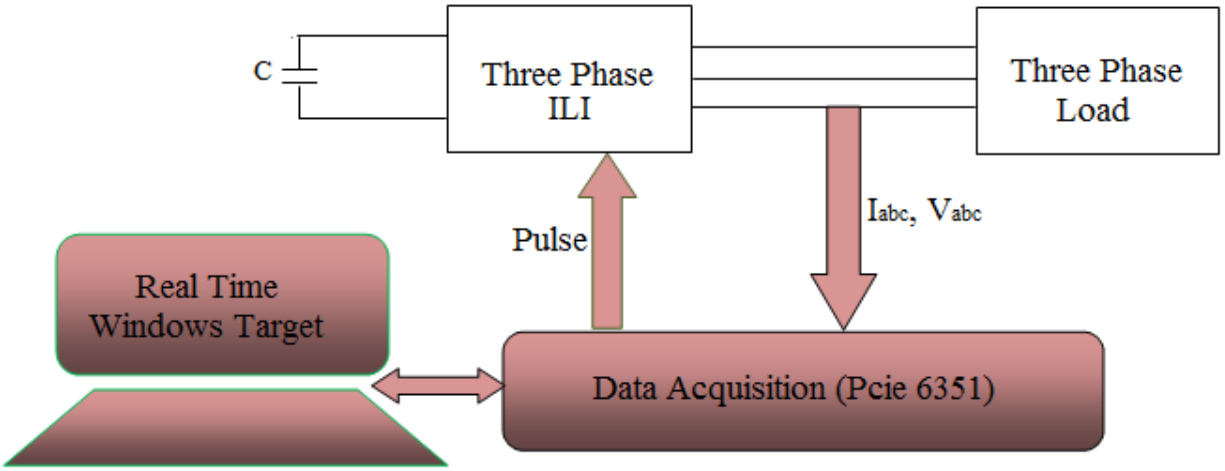

Figure 7.7 Control scheme and experimental set up

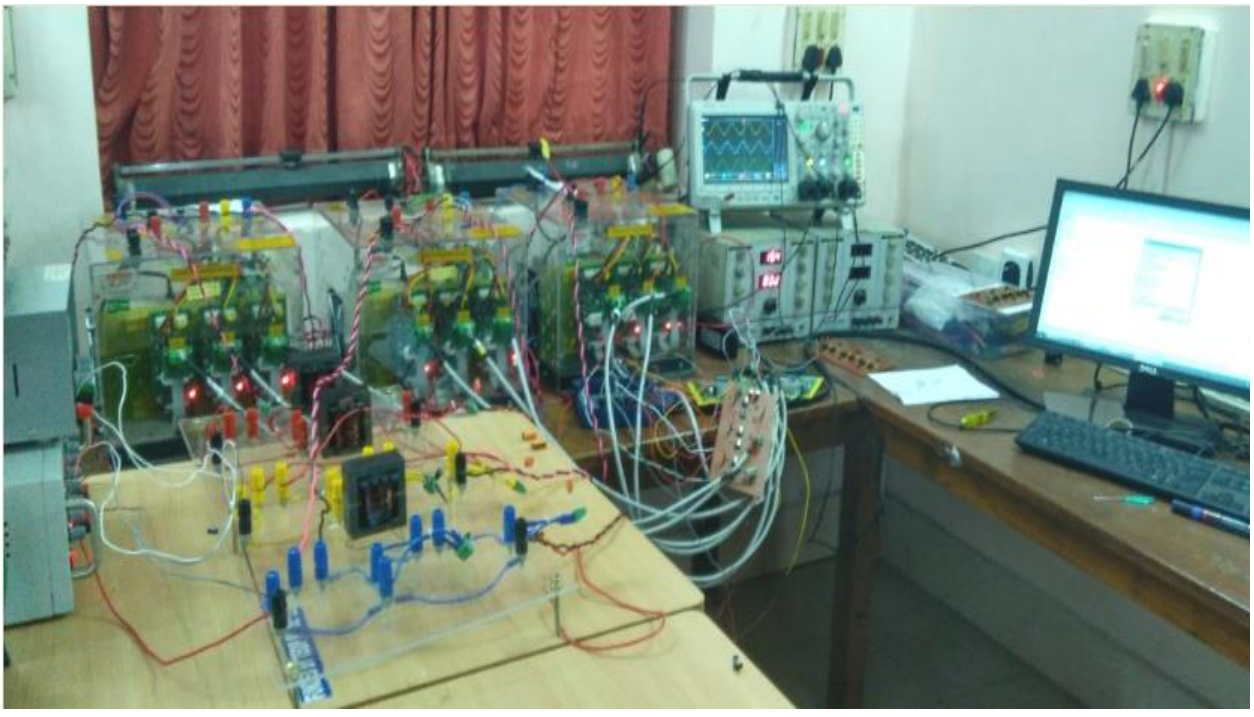

Figure 7.8 Photograph of the Hardware set up

7.5 Experimental Results

In this work, the performance of single-phase ILI and three-phase ILI topologies have been experimentally verified. The control logic of proposed inverter based on fully rectified PWM is

implemented by MATLAB/Simulink and corresponding C-code file utilizing code composer studio (CCS) development environment. This programme code has been transferred through multifunction I/O device (SCB-68A) by interfacing cable from PC. The gate pulses are available at SCB-68A is approximately 3.3V which is not sufficient to drive the IGBT modules. To strengthen the gate voltage level from 3.3V to 15V a level shifter is used and it act as a buffer circuit and provides the appropriate gate voltage level to the IGBT stack. The PCIe-6351 card generates one/three high frequency fully rectified PWM signals with respect to single-phase ILI and three-phase ILI topologies. Through hysteresis current controller, the switching signals to the IGBTs gate are passed to generate fully rectified sinusoidal voltage output waveform across the buck output terminals. In the H-Bridge topology, four switches are arranged in a complimentary manner. In each arm, each pair of switches are turn ON/OFF with a finite period 0.01s. Consequently, fully rectified sinusoidal waveform is converted into a sinusoidal waveform at desired frequency and then supplied to the load.

The load current is measured under steady state condition using a current sensor with ratio of 100 mV/A in each phase, and load voltage is measured by means of voltage sensor LV-25-1000. Figure 7.9 shows the hardware output voltage waveform across the buck capacitor and figure 7.10 shows the voltage across the load resistor of single phase ILI and the corresponding gate pulses. Figure 7.11 shows the hardware output voltage waveform across star connected resistor load of three-phase ILI and the output voltage and current are shown in figure 7.12.

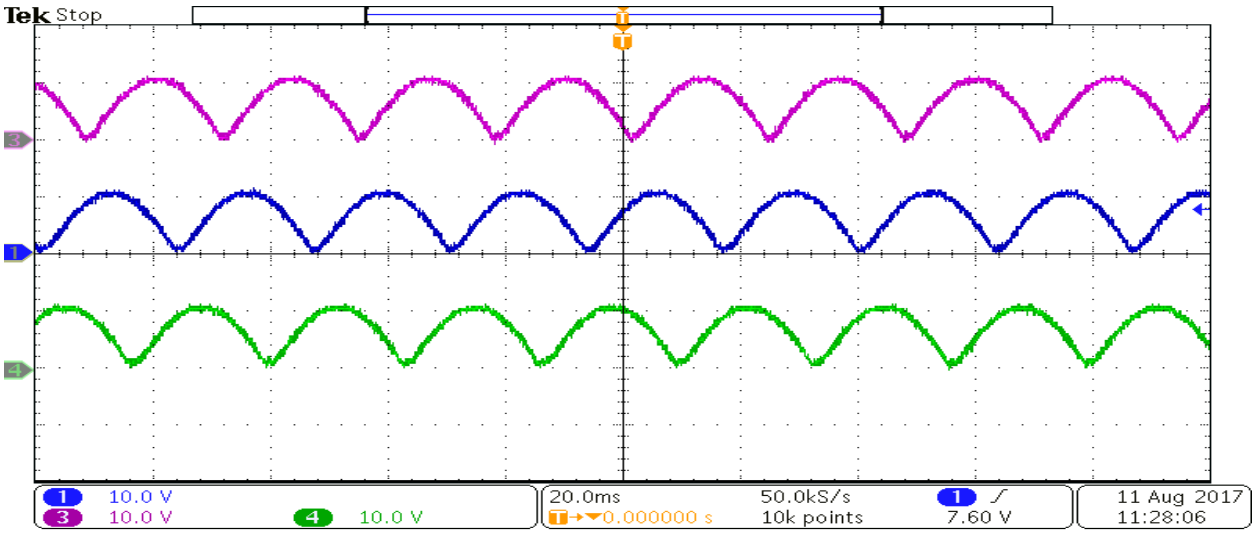

Figure 7.9 Three-phase buck output voltage

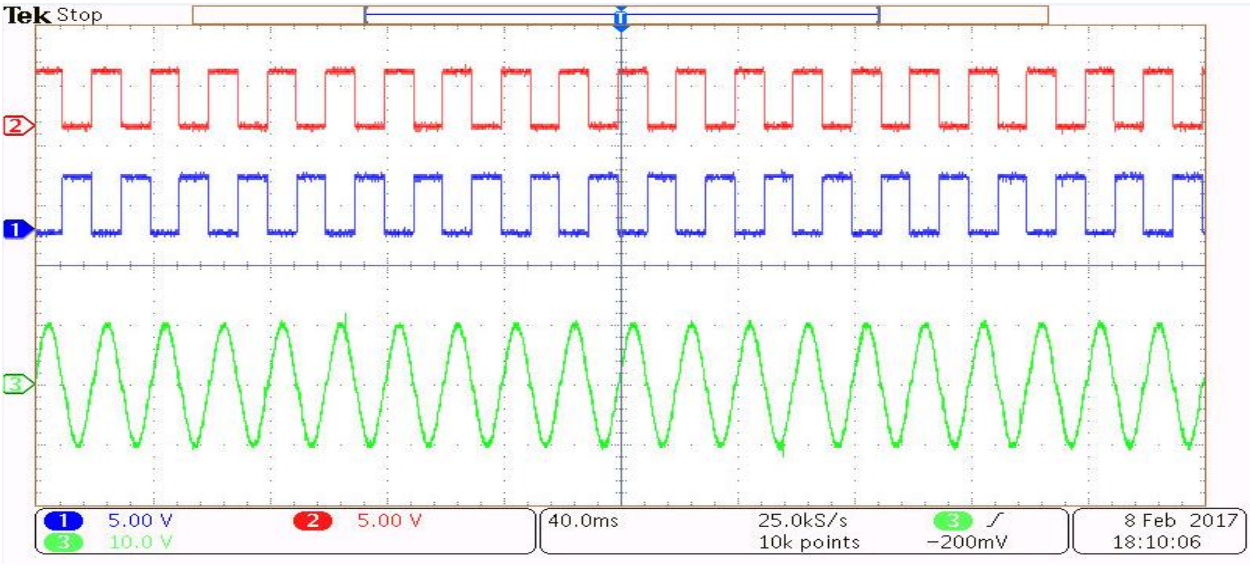

Figure 7.10 Fundamental output voltage waveform and gate pulses to H-Bridge

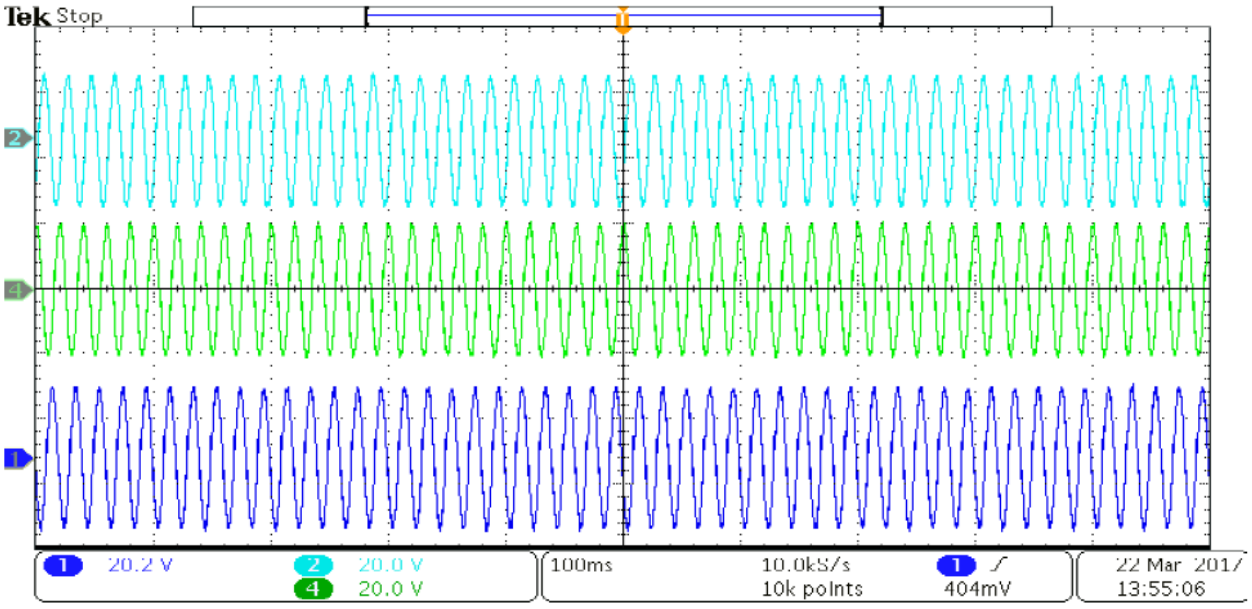

Figure 7.11 output voltage waveform across star connected R load in three-phase ILI

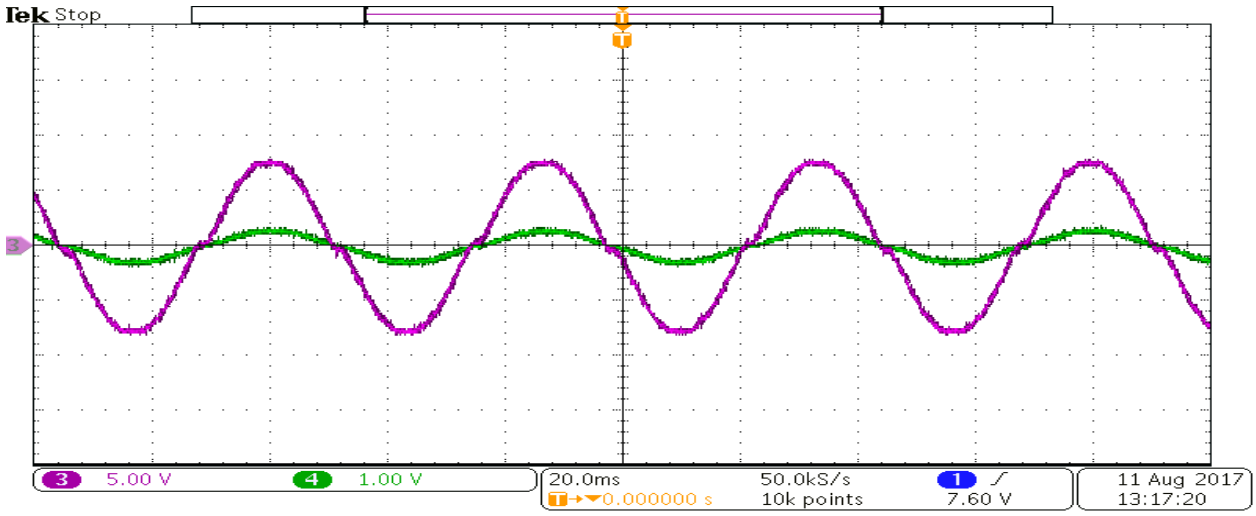

Figure 7.12 Output voltage waveform and current waveform across R load in a Single Phase ILI

Next stage of hardware implementation was to use this ILI circuit to compensate for reactive power and harmonic filtering. Laboratory setup of proposed DSTATCOM circuit is implemented in the laboratory. It is fed to a local grid with nonlinear loads nearby. A capacitor is connected as the input to the system. The initial voltage of the capacitor is taken from a rectifier. Different values of this voltage is applied and observed the system performance. The injected current is measured and compared with the reference current calculated. The dc voltage varied from 50 to 100 volts and source voltage varied from 40 to 80 volts. The current injection transformer is used to inject the inverter current into the point of connection and the coupling reactor of reactance 5 mH is used. The three-phase non-linear load currents, and phase voltages are sensed using current and voltage transducers. These values are given to data acquisition card using national instruments BNC-2120 cable. The preset value is calculated by using these sensed voltages and currents. Control signals are attained via Simulink desktop Real Time Windows Target (RTW) environment using Multi-function I/O device and Data Acquisition (DAQ) card NI PCIe 6351. The sensed value of the converter is 0.7 ampere which is same as the estimated reference current value as shown in figure 7.13. The experimental waveforms of reference current, actual inverter current and source voltage and current for one phase of an infinite level inverter based DSTATCOM are shown in figure 7.13. Figure 7.13 (a) is the reference and tracking currents of the proposed system and figure 7.13 (b) shows the source voltage and source current after compensation. In the infinite level inverter, the amount of harmonics is inversely proportional to

switching frequency. In the present system, developed using IGBT, the operating frequency is limited to 10 kHz. The source voltage and current are monitored and found that these are exactly in phase and hence unity power factor is obtained. So, this new ILI based DSTATCOM topology exhibit better performance as harmonics and reactive power compensator. The source voltage and current are in phase and hence unity power factor is obtained.

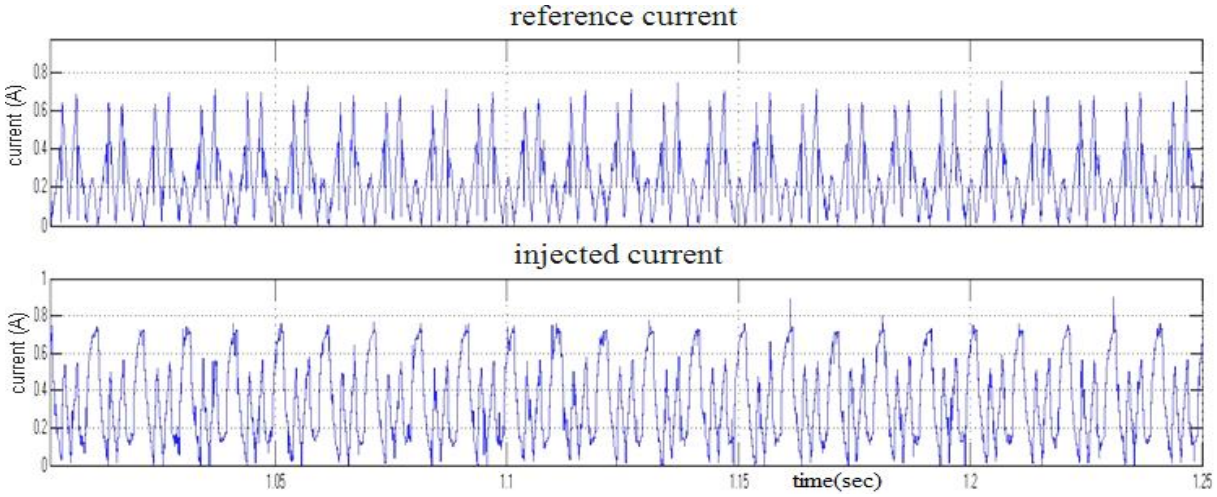

Figure 7.13 (a) Reference and inverter currents of the compensator

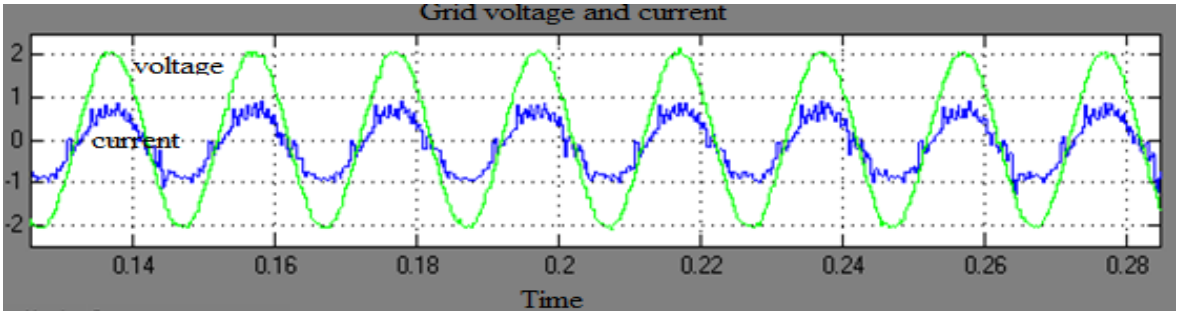

Figure 7.13 (b) Experimental results of source voltage and current

7.6 Summary

In this chapter experimental set up and experimental results of ILI based DSTATCOM are discussed. The hardware model of three-phase ILI is developed in the laboratory using National Instrument's DAQ card and connector and using the ILI circuit developed, DSTATCOM is developed in the laboratory and compensation performance of the ILI is analyzed. The grid voltage and load currents are sensed using voltage and current transducer respectively and the

reference current is calculated in the Matlab /Simulink Real Time Windows target. The calculated and measured reference currents are exactly same. The source voltages and currents are in-phase and thus unity power factor is obtained. The experiment is carried out with non-linear loads nearby. The experimental setup is tested for harmonic filtering and reactive power compensation. It also tested experimentally at different operating conditions to observe the reliability of the proposed system. The ability of this proposed system to track the reference current is excellent. It is also an excellent remedy to mitigate harmonics and to compensate reactive power. Since ILI utilizes just one high frequency power semiconductor device in each phase, the switching power losses are decreased largely and has a merit of avoiding shoot-through problem.

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Chapter 8

Conclusions and Future Work

8.1 Introduction

A three-phase switched mode dc-dc converter based dc-ac converter with feedback controller was developed for working as DSTATCOM. It has infinite number of voltage levels depending on the carrier frequency used and hence the name Infinite Level Inverter (ILI). Along with the current reference extraction algorithm, the inverter system could act as a DSTATCOM and compensate for non-linear and reactive loads affixed to the point of coupling. Fixed band hysteresis current controller was used for the operation of this inverter as DSTATCOM. A single proportional plus integral (PI) controller used in the system could control the grid current and regulates the dc-bus voltage. It also enabled fast dynamic response. The reactive power control and harmonic filtering was carried out using MATLAB/Simulink and the hardware model of the system is developed using National Instruments PCIe card.

The increased penetration of non-linear loads and distributed generation sources in the distribution system contributes to the power quality issues. The effects of nonlinear loads and different types of power quality enhancement solutions were reviewed. Various Flexible AC Transmission Systems for DSTATCOM applications and its present scenarios were reviewed. Among the various types of power quality compensation techniques, FACTS device was found as the most suitable candidate to enhance the quality of power. For proper compensation in the distribution system, the selection of voltage source inverter played a very significant role in terms of power loss, efficiency, cost and total harmonic distortion. Various inverter configurations and control schemes suitable for DSTATCOM applications were presented in the literatures. Multilevel inverter topologies are capable of producing a higher output voltage levels with the cost of higher number of switching devices. The characteristics of inverter topologies were studied from their application point of view. The power quality enhancement with the major types of MLI topologies were analyzed in

detail. The cost, losses and size reductions with utilization of MLI topologies were mentioned. Also, the merits and demerits of conventional voltage source inverter topology as well as MLI topologies were presented. Various configurations of such systems with several parameters were compared. Further different types of reference current extraction algorithms were considered for review. Various control methods were found in the literature to achieve the grid ancillary services.

8.2 Summary and Major Findings

The review of existing topologies and its control has led to the scope of introducing more simplified and efficient inverter structure for DSTATCOM application. The synchronous reference frame strategy and the instantaneous reactive power theory are the promising methods that can be used for the generation of reference current. The single PI controller used in the proposed system was able to regulate the dc-bus voltage and grid current. By applying SRF current reference generation algorithm, the dynamic performance of the complete system is improved. Also the system was operated under constant switching frequency.

8.2.1 Modelling and analysis of VSI based DSTATCOM

Analysis of DSTATCOM using traditional voltage source inverter was carried out with two types of current extraction algorithms namely IRPT and SRF algorithms. The simulation analysis was carried out by modelling each and every component of the system such as current reference generation algorithms, current controller, distribution line, load etc. Mainly the THD factor of grid current and voltage was observed. The source side harmonics were high in IRPT algorithm. DSTATCOM using SRF strategy gave better performance than IRPT algorithm in terms of source current harmonics. The dc-link voltage requirement for the DSTATCOM operation was found 680 volts. Constant hysteresis controller was implemented with simple comparator.

8.2.2 Modelling of Infinite Level Inverter

Operating principle of the three-phase ILI was explained and its mathematical equations were derived. The three-phase infinite level inverter topology was a switch mode inverter based on reducing number of passive devices and high frequency active switches compared to multilevel inverters. It consists of a single high frequency switch in each phase that results reduced switching power loss thereby increasing the overall efficiency of the system. Absence of shoot

through menace eliminated the dead time requirement. The ILI produces a sinusoidal voltage that can be used in power system and other applications. It is most suitable for continuous operation, compensation, control for reactive power requirements and voltage control. The output ac voltage of this inverter can be controlled theoretically any value between zero to infinity. It was found that the dc voltage required to generate three-phase voltage of 400 volts was theoretically 325 volts thereby ensuring high dc-link utilization. It also offered reduced losses, minimized operating costs and improved reliability. THD analysis was carried out for different loads and found very low value of source current THD especially for RL load that was below 1 %. The proposed inverter topology offered better system reliability that facilitates the use of this topology for critical loads. This topology had numerous benefits over traditional inverter topologies.

8.2.3 ILI as DSTATCOM

The three-phase ILI topology was used for DSTATCOM application. The performance of ILI as DSTATCOM was analyzed. Among the various performance indices, the switching loss, dc-link voltage requirement and the THD factor of source current were observed. It was also obvious that the fundamental output voltage obtained from the proposed infinite level inverter based DSTATCOM required less DC voltage with very high dc-link utilization. This DSTATCOM exhibited superior performance with the d-q control strategy. The source current and voltage THD were very low and the dc-bus voltage requirement for the DSTATCOM performance was reduced by 50% as compared to traditional VSI based one. As a result, the cost, size and weight can be reduced. Additionally, any small sized capacitance can be used for the implementation. This system avoided the use of additional LCL filters and line frequency transformer. The system consists of a single PI regulator to operate in all possible modes with less transients in terms of settling time and maximum overshoot. Hence the entire set up was found effective in compensation performance.

8.2.4 ILI as PV-DSTATCOM

The infinite level inverter was used to interface solar photovoltaic system into the distribution network and to compensate for the reactive and harmonic currents required by the non-linear load with the presence of PV in the distribution network. The PV system was modelled as single diode model. The control system used to control the PV-DSTATCOM system was same as that used for

ILI-DSTATCOM. The power quality enhancement performance of the PV-DSTATCOM was found satisfactory. The FFT analysis showed that the THD was within the limit. It also had all the advantages of ILI such as reduced THD, minimized switching power losses and improved response. Its greater dc-bus utilization minimized the voltage stress across the switching devices. The simulation results proved that the PV-DSTATCOM was very successful in obtaining high quality output waveform with lower THD.

8.3 Major Research contributions

The research work analyzed the effects of new three-phase infinite level inverter as DSTATCOM. The ILI based DSTATCOM set up was modeled with a simple loop controller. The proposed topology and compensation performances were verified by simulation and experiments. Both simulation and experimental results showed that the proposed inverter and compensation modes can effectively enhance the reliability and utilization of ILI DSTATCOM, and had great practical prospective. From the simulation and hardware results, it was understood that it could compensate for both reactive power and harmonics with fast dynamics. It also supported the distribution network with renewable energy sources like solar PV.

The major research contributions can be enumerated as below

- An infinite level inverter for DSTATCOM application was developed that has the capability to compensate for major power quality issues such as reactive and harmonic current.
- The THD of source current and voltage of ILI based DSTATCOM set up could be reduced with synchronous reference frame strategy and fixed band hysteresis current controller.
- It was found that the switching loss of this DSTATCOM system was low and improved the effectiveness as compared to traditional voltage source inverter based DSTATCOM.
- The ILI based DSTATCOM system with a single PI controller could able to manage reactive and harmonic power compensation in PV supported distribution network.
- ILI based DSTATCOM with PV as DC source was analyzed.
- High value of dc-link utilization was achieved using this topology and hence the switching stresses were greatly minimized.

- The capacitor voltage required was just 360V in order to attain a peak value of 630V and rms value of 440V. So, High value of dc-bus utilization was achieved using this topology and the voltages across the switching devices were greatly minimized.

8.4 Limitation and future work

The thesis work concentrates only on the operation of the three-phase ILI as DSTATCOM including PV fed distribution system for reactive power compensation and harmonic filtering. The ability of the ILI to operate as a DSTATCOM was investigated using simulations done in MATLAB/Simulink environment. This ILI can also be used to integrate other renewable energy resources such as fuel cell, micro turbines, wind power and to control the active power transfer between the DG units and the grid. The ILI based DSTATCOM system considers the added functionalities of reactive power compensation, unity power factor operation and harmonic compensation. The system can be extended with add on functionalities like reactive power support for the grid to keep the supply voltage at a fixed value, frequency regulation and so on. Also, this infinite level inverter based system can be utilized for electrical vehicles. Considering the efficiency and simplicity in implementation of the prototype, a low power model was used in the work. The same control board could be used with large power circuit to verify the different modes of operation of the system as a future work. Furthermore, this system can be used for the power quality enhancement of a transmission network. It can be of significant interest in the area of power electronics since a reliable and efficient system which produces minimum THD can be put into use in various applications. Due to the inherent advantages of the proposed system, implementation of ILI based power electronic system can be promising in the near future.

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List of Publications

Journal Publications

1. V Renukadevi, B. Jayanand., and M.Sobha, "A DC-DC Converter based Infinite Level Inverter as DSTATCOM", International Transactions on Electrical Energy Systems (2018)., DOI: 10.1002/etep.2724., Impact factor 1.084. (wiley).

2. Renukadevi. V and Jayanand. B, "Infinite Level Inverter based Single Phase Active Power Filter", International Journal of Advanced Research Trends in Engineering and Technology (IJARTET) Vol. 4, Special Issue 6, April 2017.

3. Renukadevi. V, Jayanand. Band M Sobha, " *PV DSTATCOM* - a new Inverter for reactive power control in PV fed distribution network" Journal of Renewable and Sustainable Energy (under review)

Conference Publications

1. Renukadevi V, Jayanand B “Harmonic and Reactive power compensation of Grid connected Photovoltaic system”, International Conference on SMART GRID Technologies, Elsevier, August 2015, pp. 438-442.

2. P S Athira; V Renukadevi; B Jayanad, “Infinite Level Inverter based DSTATCOM for power quality enhancement”, IEEE-International Conference on Smart Technologies for Smart Nation, 2017,DOI-10.1109/SmartTechCon.2017.8358567.

ABOUT THE AUTHOR

Renukadevi V was born at Kodumbu village in Palakkad district in 1978. She had her B. Tech in Electrical and Electronics Engineering from Government Engineering College Thrissur, Kerala in the year 2003 and took M. Tech in Power Systems from the same College in 2010. She is being actively participated in various academic activities. She worked as Assistant Professor in Electrical and Electronics Engineering Department of Prime College of Engineering from July 2010 to July 2013. She also has five years of industrial experience as Electrical Engineer. She joined as a full time research scholar under CERD fellowship in the Department of Electrical and Electronics Engineering, Government Engineering College Thrissur in August 2013. She had presented several papers in National and International conferences. Major area of interest includes Power Electronics, Distributed Generation, Power Quality etc.

Permanent Address:

Karakkad (House)

Karingarapully (PO)

Palakkad, Kerala, India.

Pin: 678551.